10T and 8T Full Adders Based on Ambipolar XOR Gates with SB-FinFETs

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***Abstract*—We introduce novel ten (10T) and eight (8T) transistor full-adder logic gates based on recently proposed gate work-function engineering (WFE) approach. When applied to sub-10 nm Schottky-barrier (SB) independent-gate FinFETs, WFE leads to hitherto unexplored 4T and 3T XOR implementations that operate with either only one or no inverted input, respectively. The novel 4T and 3T XOR gates eliminate the need for inverted inputs provided that ambipolar I-V characteristics is shifted by the associated gate work-function in the right direction, where another conduction channel exists. Following the logic verification of the novel 4T and 3T XOR gates via TCAD simulations, we then continue to show how these novel gates can be put to use in building ultra-compact 10T and 8T full-adder circuits, which would normally require up to 20 FinFETs in conventional CMOS architecture. Simulated power-delay products of the novel full-adders show significant ($\sim 5\times$) improvement in dynamic performance attributed largely to the 50% reduction in total area as well as parasitics, at the expense of loss in noise margins. Besides the full-adders explored, the presented WFE approach could in general provide area and performance gains also for other logic building blocks that can be redesigned using SB-FinFETs.**

I. Introduction

As silicon-based CMOS technology is searching for alternative devices and approaches to extend its dominance and delay the imminent demise of Moore's scaling, minimal changes to the established FinFET architecture is welcomed due to associated cost savings and rapid adaption cycle [1], [2]. Although less revolutionary, this "more-of-Moore" approach can provide additional time for such paradigm-shifting alternatives to Si CMOS to be fully developed. Recently, we proposed such an effort to extend conventional FinFET based logic down to 5nm via gate workfunction engineering (WFE) [3], which resulted in ultra-compact XOR/NAND/NOR logic gates with significant (~50%) reduction in area and power-delay-product. In the proposed gates, the WFE is selectively applied to Schottky-barrier (SB) FinFETs with independent gate inputs, which leads to entirely novel logic elements such as 1T CMOS pass-gates as well as 4T XOR gate and 2T NAND/NOR gates with non-inverting inputs. In the present paper, we further extend the WFE approach on SB-FinFETs and introduce additional designs for ultra-compact 4T and 3T XOR gates with one or no inverting inputs, respectively. In turn, we also illustrate how the compact XOR and 1T pass-gate designs can be conveniently utilized to built novel 10T and 8T CMOS full-adders that have never been explored before.

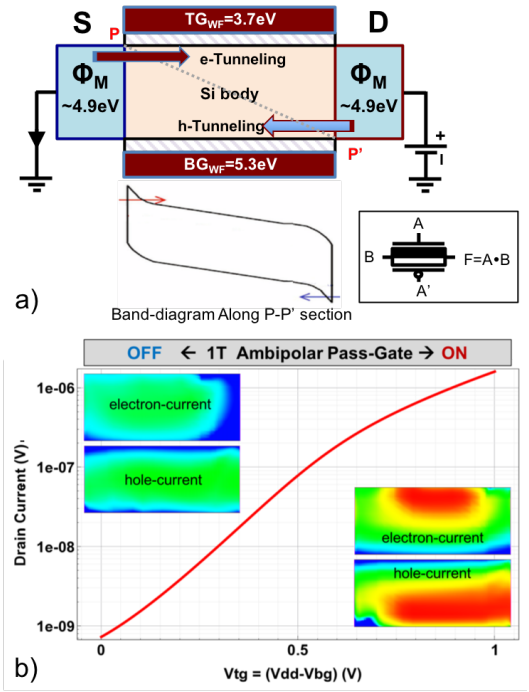

Fig. 1. Proposed 1T pass-gate based on independent SB-FinFET optimized for dual channels: a) Bottom gate for hole tunneling/conduction and top gate for electron tunneling/conduction;, b) simulated characteristics of the 7nm pass-gate and the corresponding e/h current densities in ON and OFF cases (insets) for V_{ds}=1.0V bias

The main building block of the proposed compact logic gates is the generic ambipolar SB-FinFET transistor (t_{ox}=1nm, ϵ_{ox}=12, t_{Si}=4nm) with SB source/drain contacts, capable of working both as a p- or n-type MOSFET in CMOS gates, as shown in Fig.1a. An ambipolar device can inject both electrons and holes into the undoped channel, hence have two conduction modes, depending on the size of Schottky-barrier height dictated by the choice of S/D contacts. The presence of SB at the contacts 'lifts-up' the potential at the end of the channel that would otherwise slip away from gate control due to depletion fields of S/D junctions, thus improving device scalability. With the correct contact metal choice, it can deliver equal current drive for both types of carriers [4], [5] and has

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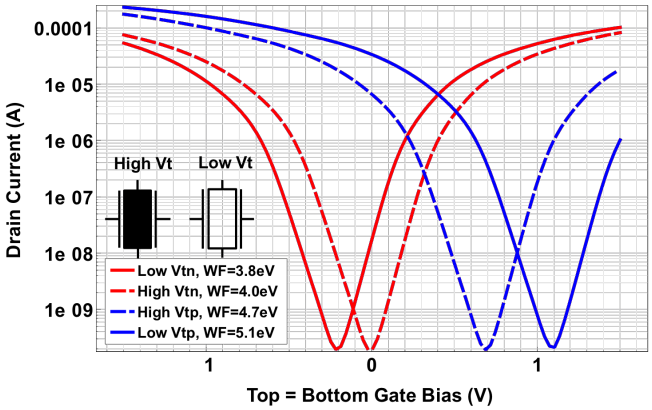
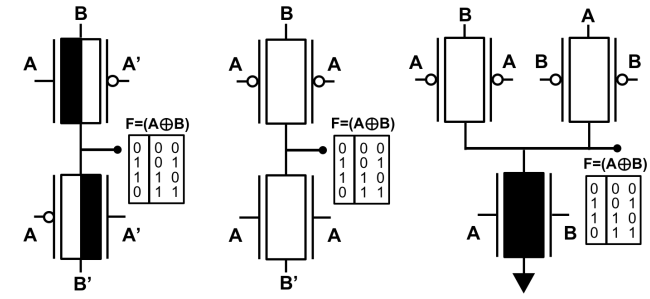


Fig. 2. I-V characteristics of ambipolar FinFETs optimized for low & high threshold FinfETs of both polarity. WF for S/D is 5.0 eV and TG=BG as given in the legend.



Channel	Contact	ϕ_{WF} (eV)
n	Top Gate	3.7
p	Bot Gate	5.3
n/p	Src/Drn	5.0

Device	Contact	ϕ_{WF} (eV)
nMOS	T/B Gate	3.6
pMOS	T/B Gate	5.2
n/p	Src/Drn	5.0

Device	Contact	ϕ_{WF} (eV)
nMOS	T/B Gate	3.9
pMOS	T/B Gate	5.2
n/p	Src/Drn	5.0

Fig. 3. Compact XOR gates utilizing the proposed WFE approach with independent-gate SB-FinFETs. a) 6T XOR with ambipolar CMOS pass-gate; b) 4T pseudo-CMOS XOR with n and p FinFET pass gates, and c) novel 3T pseudo-CMOS XOR with *no inverted inputs*. Note that for any inverted input a 2T CMOS inverter is needed and included in the naming convention

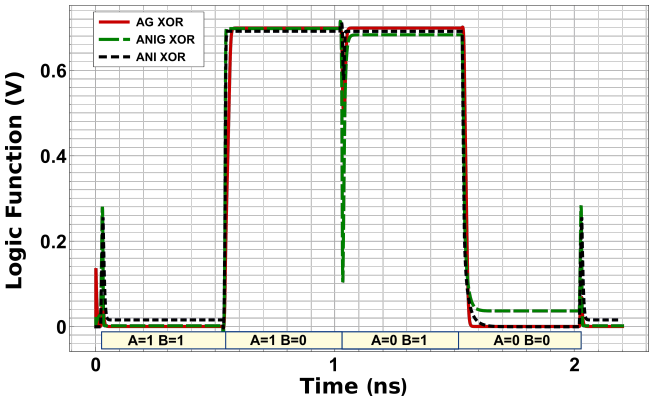


Fig. 4. Verification of ambipolar XOR functions via TCAD simulation. XOR operation is confirmed all three variants, each with unique workfunctions as indicated in Fig.3.

been suggested by several groups as a reconfigurable logic element in CMOS circuits. [6]. When realized in the form a single FinFET with *two independent gates* optimized with dissimilar workfunctions, the device can operate as 1T pass-gate with one electron and one hole channel in a single Si body [3]. It is this unique ability to set independent gate workfunctions in a single FinFET that enables us to pursue the novel circuits introduced below.

Another important capability used in the proposed XOR and full-adder implementations is the fine threshold adjustment via WFE that leads to lateral shifts in the ambipolar I-V characteristics for SB-FinFETs as shown in Fig.2. Such higher threshold FinFETs are needed to create pass-gates that only turn on when both independent gates are driven (AND function) in a single transistor, which is key to combining two series FinFETs in the NAND/NOR logic gates into one.

II. Novel 4T and 3T XOR Gates

There are three types of XOR gates that can be built via WFE optimized SB-FinFETS. The first one was introduced in our earlier work [3] and is based on the use of two ambipolar pass-gates (see AG-XOR Fig.1) driven by both inputs (A, B) as well as their compliments $(\overline{A}, \overline{B})$. When the FinFET gates are built from two different metals (possible, but not a trivial modification) with workfunctions on either side of the mid-gap value (4.6eV), there will be two opposite-type channels in a single FinFET. This is analogous to pass-gate (or transmission-gate) parallel CMOS pair with n/p-type MOSFETs driven with opposing logic states. Thus the AG-XOR requires a total of six transistors including the inverters, and only two transistors if the inverted inputs are available. In comparison, the XOR with conventional CMOS pass-gates would require 8 transistors with the inverters.

The second XOR, named ambipolar non-inverted gate (ANIG) XOR, is essentially a novel and superior implementation of standard 6T CMOS XOR [7] using SB-FinFETs optimized via the WFE approach. Instead of one nMOS and one pMOS pass-gate with individual S/D junctions, we utilize SB contacts and modify the gate workfunctions to operate either as n- or p-type pass gates. Thus, in an ANIG-XOR, A is the input and B and $\overline{B}$ drive positive and negative supplies, respectively, as shown in Fig.3. Since we utilize symmetrically driven SB-FinFETs, this device can also be built with conventional FinFETs available today, provided the workfunctions indicated in Fig.3b are adapted in the design. Like the earlier AG-XOR case, if $\overline{B}$ is already available this design culminates in a 2T-XOR implementation as well. If the inputs B and $\overline{B}$ are replaced with different logic variables, this circuit can also serve as 2-to-1 MUX, which will be useful in the full-adder carry-out calculation (see Fig.5 and Fig.7 later)

The third and final ANI-XOR (Fig.3c) is a unique and hitherto unexplored gate, composed of only three SB-MOSFETs and no inverters at all. It relies on NAND like pull-down network based on a high-V_t nMOSFET (can only turn on if A=B=1) and two low-V_t pMOSFETs for pull-up network, reminiscent of ANIG configuration. Since no inverter is needed at all, this device can ensure the lowest transistor account for logic systems where the logic inverse inputs are not readily available. It also requires two different gate workfunctions to ensure that thresholds can be optimized for each transistors.

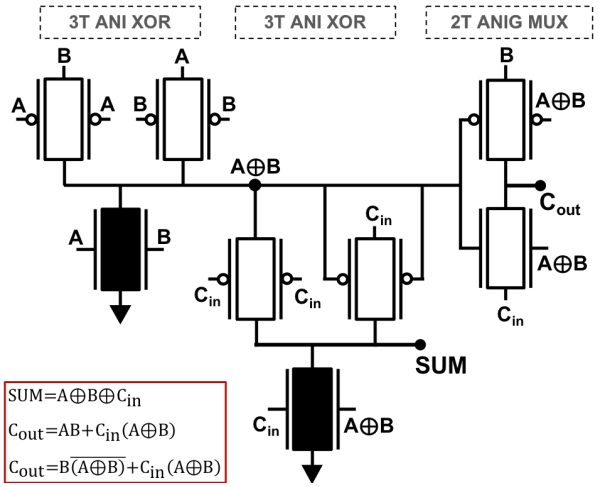


Fig. 5. Proposed 8T full adder using novel minimalist ambipolar XOR gates with no inverted inputs. For C_{out} term an identity is used to take advantage of 2T MUX that can be constructed using the 2T XOR with no inverted inputs

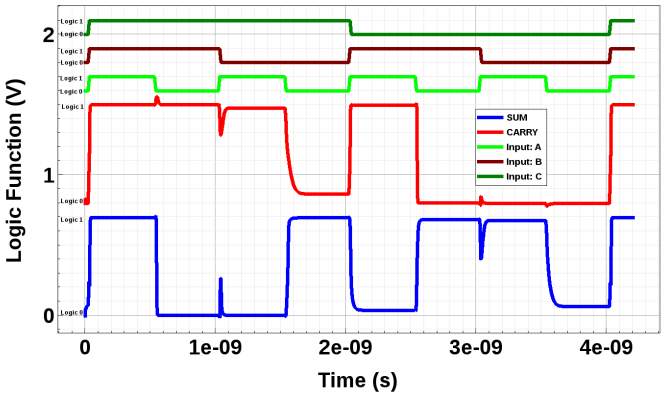


Fig. 6. Verification of operation for 8T Full-adder circuit via TCAD simulations

Fig.4 clearly shows that all of the three proposed XOR-gates operate correctly and evenly with similar rise/fall times. The glitches at the transitions are due to relatively slow (10ps) 0/1 or 1/0 edges used in the simulation to ensure fast and good convergence in the demanding TCAD simulations. AG-XOR has the best noise margins, and ANIG-XOR is the worst, especially in its pull-down network that drops $\sim 30mV$.

III. 10T & 8T Full adders via Ambipolar SB-FinFETs

Besides general logic use, XOR gates are especially important for the efficient implementation of full-adder (FA) circuits. In the present work, thanks to the novel XORs designed using WFE approach, two novel CMOS FAs are introduced for the first time. The first of these is an eight-transistor implementation, named AFA-8T (Fig.5) that requires no inverted inputs. It is based on two ANI-XOR blocks introduced earlier and a single 2T ANIG block re-purposed as a 2-to-1 MUX circuit via top and bottom inputs. Note that carry-out bit (C_{out}) takes advantage of equivalence between $A.B = B.(\overline{A \oplus B})$ so a second ANI-XOR gate can be used,

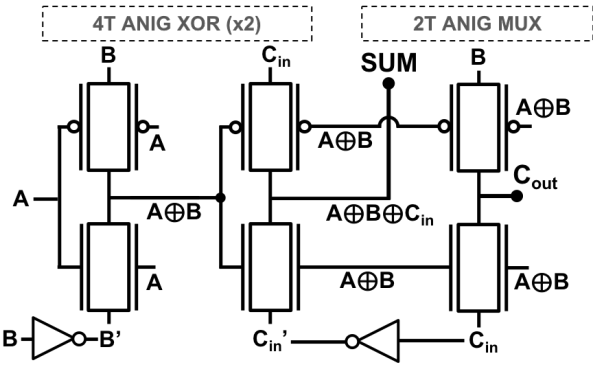


Fig. 7. Proposed 10T Full Adder using novel minimalist Ambipolar XOR gates and two additional inverters (not shown). Note that if inverted inputs are available the full-adder will require only 6T.

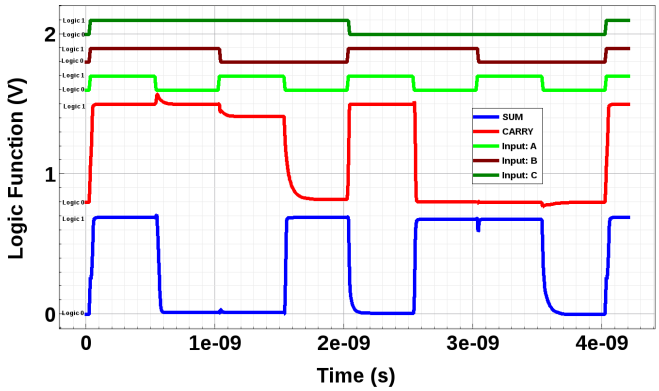


Fig. 8. Verification of operation for 10T Full-adder circuit via TCAD simulations

eliminating the need for an inverter. Operation of the FA8T circuit is verified via TCAD mix-mode simulations in Fig.6. For the chosen set of workfunctions, SUM term is working with minimal ($\sim 10mV$) loss in noise margins, whereas the carry bit has more significant ($\sim 85mV$) loss for one input combination ($A = 1, B = 0, C_{in} = 1$). This loss can be corrected if workfunctions are slightly altered. However, this may be a zero-sum game as losses may appear in other input combinations. In most cases, the culprit is the second ANI-XOR stage ($C_{in} = 1$) which inherits a slight loss of logic levels from the first XOR stage. Thus, if workfunctions for subsequent ANI-XORs are slightly varied, at the expense of process complexity, or by playing with W/L ratios in each stage, it should be possible to mitigate these losses further.

The second FA circuit given in Fig.7 is called AFA-10T, since it requires ten transistors to function, including the two inverters. Thus if inverted inputs are available, it would take only 6T to operate this FA design, employing only two 4T ANIG-XOR stages introduced above. Its operation is also verified via TCAD simulations as shown in Fig.8. Unlike the AFA-8T design, both sum and carry outputs suffer from $\leq 60mV$ losses in noise lower margins, while smaller losses also visible in the logic high state, indicating that the work functions chosen for the correct XOR operation may still be suboptimal.

IV. Discussions

Although 3T & 4T CMOS XOR gates are reported in the literature [8], [9], they rely on nMOS or pMOS *only* pass-gates that does not pass logic-0 or logic-1 states equally well. As a result, they would require additional inverting buffers to restore logic levels at their outputs, especially in multi-stage logic functions. If conventional CMOS pass-gates, built from parallel connection of an n- and p-type MOSFET, were to be used, noise margins can be improved at the expense of area (8 transistors) and/or power dissipation. The proposed WFE-optimized 4T and 3T XOR gates utilize full CMOS blocks that can pass logic 0/1 levels either equally well or better than single-gate counterparts owing to dual-gate action of the FinFET. Hence the present work is valuable and unique in two different aspects as it introduces two novel XORs (4T and 3T) and two full adders (8T & 10T), both based on novel WFE-optimized SB-FinFETs. To our best knowledge, the 8T full-adder proposed here is the first *fully-CMOS* logic block of its kind, as compared to nMOSFET-only example proposed earlier, which clearly had *significant* loss of noise margins that would disqualify it in real applications [10]. Similarly, ANI-XOR proposed is the first CMOS logic gate that deliver XOR function using only three transistors and no inverters.

TABLE I
SWITCHING PERFORMANCE OF THE PROPOSED ULTRA-COMPACT FULL ADDERS BASED ON AMBIPOLAR SB-FINFETS AS COMPARED TO THE CONVENTIONAL CMOS PASS-GATE DESIGNS WITH 20 TRANSISTORS

Logic Gate	$< P >$ [nW]	$< t_d >$ [ps]	$< PDP >$ [aJ]	NM Loss [mV]
$AFA - 8T_{SUM}$	470	27.94	13.13	60
$AFA - 8T_{Cout}$	261	29.06	7.57	60
$AFA - 10T_{SUM}$	197	17.59	3.46	85
$AFA - 10T_{Cout}$	1206	4.26	5.14	20
$CMOS - 20T_{SUM}$	7002	4.61	32.25	10
$CMOS - 20T_{Cout}$	6510	5.10	33.21	5

Besides the obvious area gains approaching 50%, the proposed FA designs offer significant gains in dynamic performance. This may be ascertained by comparing its power-delay product (PDP) with the conventional CMOS designs, as provided in Table I. *Total* PDP of the AFA-8T & AFA-10T cases are found to be 8.6 aJ and 20.6 aJ, as opposed to the conventional CMOS FA design with PDP of 65.5 aJ. While these values are not accurate given the finite parasitics included in the TCAD model ($R_{S,D} = 50$ Ohms and $C_L = 1fF$) and lack of gate tunneling in the present model, they do indicate a very competitive performance for the proposed FA circuits. However, the noise margin losses are greater in the proposed FAs, which needs to be improved further, possibly by fine tuning the workfunctions and Fin dimensions. Doing so will most likely lover power dissipation and enhance the PDP even higher. Instead of the XOR gate level, such additional optimization of workfunctions might be more beneficial at the functional level, (i.e.) altering the workfunction of a specific transistor so as to improve overall FA performance, an approach currently being studied and to be reported in a separate publication.

V. Conclusion

A novel approach to design ultra-compact full adders in sub-10nm CMOS was proposed and verified via TCAD simulations. The approach utilizes work-function engineering of independent-gate Schottky-barrier FinFETs to build three unique XOR gates, including a never-reported-before three-transistor gate (3T NI-XOR) requiring no inverters. Based on these novel XOR gates, two different full adder circuits have been developed that require only 8 or 10 transistors. While the former AFA-8T circuit requires no inversion of inputs, hence smaller, the latter could be operated with only 6T if inverted inputs exist. All gates have been confirmed via standard Synopsys TCAD tools and found to have competitive PDP at 10^{-17}J scale, which is $\sim 5\times$ lower than the CMOS counterparts evaluated in the same framework.

VI. Acknowledgement

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