4-Input NAND and NOR Gates Based on Two Ambipolar Schottky Barrier FinFETs

Talha Furkan Canan,
Savas Kaya, Avinash Karanth
School of Elec. Eng. & Comp. Sci.
Ohio University, Athens, OH 45701, USA
Email: {tc675716, kaya, karanth}@ohio.edu

Ahmed Louri
Dept. of Elec. & Comp. Eng.
George Washington University,
Washington, DC 20052, USA
Email: louri@email.gwu.edu

***Abstract*—We report on four-input NAND and NOR gates using only two 7nm Schottky-Barrier (SB) independent-gate FinFETs transistors that take advantage of gate workfunction engineering (WFE). Careful optimization of workfunctions at the source/drain contacts as well as two independent gates of the SB-FinFETs provide unprecedented control of the threshold in the ambipolar device operation. It is used in this work to tailor 4-input NAND and NOR functionalities out of only two transistors (2T), utilizing only two different metal workfunctions in a given gate. Correct operation of multi-input gates for supply voltages as low as V_{DD} = 0.5V has been verified using 2D TCAD circuit simulations. Switching performance of the proposed 4-input gates indicate that they have 45% reduction in power·delay product (PDP) as compared to the conventional 16T FinFET counterparts, which is due to substantially lower power dissipation at the expense of slower transitions. A JK Flip-Flop circuit is designed using the proposed four-input NAND gate that illustrates its advantages for the logic operation.**

I. Introduction

Multi-input logic gates are required for many applications in modern CMOS topologies including ALU optimization, secure hardware and neuromorphic computing. [1]–[4] One common method to construct these gates is to use multiple cascading stages of standard two-input gates such as four-transistor (4T) NAND, NOR and 6T XORs. However, multiple stages introduce an important amount of propagation delay, area and power overheads as well as undesired parasitics to the VLSI design. It is possible to build n-input ($n \geq 2$) one-stage gates using standard CMOS static or dynamic logic libraries. Yet, these always result in n-series transistors in the pull-up or pull-down networks that introduce large series resistors and/or require large (> 0.7V) supply voltages incompatible with the nano-scale CMOS standards. Designs based on floating-gate or floating-body CMOS devices can offer alternative solutions that trade the circuit complexity with fabrication and processing challenges of their own. [5], [6] Even more exotic solutions such as Threshold-Logic circuits require very large input stages or clocked-output comparator circuits that ultimately would not be competitive with the compact CMOS logic gates in terms of area, power and/or delay. [7] Hence, there is a clear benefit, especially in sub-10nm CMOS that can no longer scale device sizes, from the use of compact multi-input logic gates that avoid high parasitics and large supply voltages. We propose such a design here by the use of gate workfunction engineering (WFE) of Schottky-Barrier (SB) FinFETs introduced recently. [8], [9]

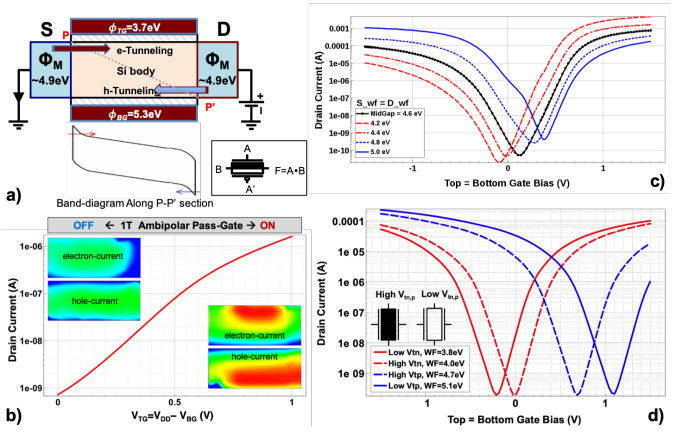

Fig. 1. Work-function engineered independent-gate SB-FinFETs [8] are used as building blocks of the reconfigurable logic gates. a) Simplified device structure and band diagram; b) ON/OFF characteristic of 1T pass-gate and the corresponding e/h current densities, c) Ambipolar I-V characteristics of the 7 nm SB-FinFET as a function of contact work-function and d) hi/low threshold ambipolar SB-FinFETs based on changes in gate workfunction

In the following, we will provide a brief overview of WFE approach as applied to the SB-FinFETs, followed by a description of ultra-compact four-input two-transistor NAND and NOR circuits based on these novel device architectures. We conclude with a demonstration of their benefits in designing a J-K flip-flop circuit. Logic verification of the proposed circuits and their switching performance are also provided along with the CMOS counterparts for comparison.

II. SB-MOSFETs & Work Function Engineering

The SB-FinFETs (L_g=7nm, t_{ox}=1nm, ϵ_{ox}=12, t_{Si}=5nm) used in the design of multi-input logic circuits proposed in this work are identical transistors except their gate metals. A generic model of the SB-FinFET is provided in Fig.1a, which are modeled using Synopsys Sentaurus simulator that employ a modified Drift-Diffusion model with Density-Gradient formalism for first-order quantum corrections as well as non-local barrier tunneling and thermo-ionic emission. Different gate metals having different workfunctions lead to different gate barrier heights shifting the threshold voltages in these

978-1-7281-6044-3/20/$31.00 ©2020 IEEE

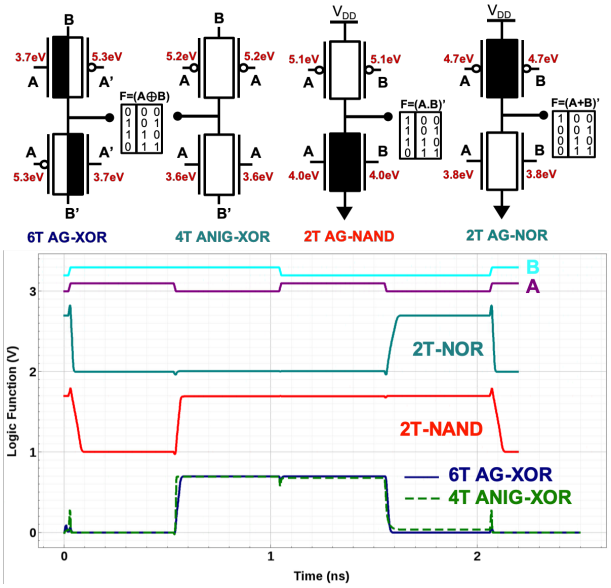

Fig. 2. Minimalist static NAND/NOR/XOR gates utilizing the SB-FinFETs engineered with independent gates and unique workfunctions (top) and the resulting logic verification via transient TCAD simulations. Excluding the inverters for the inputs, each design would require only two transistors. Solid filling indicates transistors with higher thresholds.

transistors. Moreover, workfunction tuning is also employed at the source and drain contacts of the ambipolar SB-FinFET transistors. As a result of this careful optimization, it can inject both electrons and holes into the same undoped body (Fig.1b), hence supporting two conduction modes in a single transistor (1T) CMOS pass-gate, depending on the size of Schottky-barrier height selected. The choice of SB at the contacts is critical for device operation and scalability: With the correct contact metal choice, it can deliver equal current drive for both types of carriers, as shown in Fig.1c. [10], [11] Moreover, the workfunctions of the two *independent gates* can be also optimized such that SB-FinFETs can also operate with low or high threshold devices (see Fig.1d) either with symmetrical or independent gate bias. It is this unique combination of capabilities, namely balanced electron and hole injection into two parallel channels packed into a single FinFET body and independent adjustment of gate workfunctions and channel thresholds that enables us to obtain four-input NAND & NOR gates as introduced below. Clearly, the WFE approach will require additional non-trivial processing steps, which are relatively smaller than alternative approaches and can be justified by the significant gains in area and power [9].

Based on such relatively simple yet fundamental optimization of SB-FinFET thresholds via WFE, it is possible to demonstrate minimalist 2T NOR/NAND/XOR gates and logic blocks (*excluding inverted inputs of XORs*), as explored in recent works. [9] These static CMOS gates are briefly re-introduced in Fig.2, along with their logic characteristics obtained via TCAD simulations. They illustrate that by assigning a maximum of two or three workfunctions in the SB-contacts and gate metals of FinFETs, it is possible to

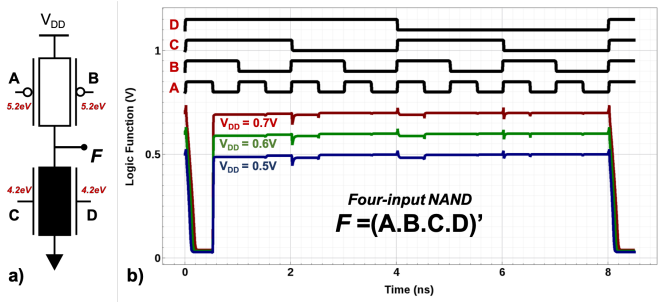

Fig. 3. a) Proposed ultra-compact (2T) four-input NAND circuit using SB-FinFETs employing WFE and b) the corresponding logic verification via TCAD simulations.

design absolutely smallest logic gates in terms of transistor counts and area. These savings translate into reduced power consumption and parasitics in these novel gates such that they possess PDP figures similar to the conventional FinFET counterparts, despite being slower in switching as independent gate configuration always lead to lower transconductance (g_m). Such trade-off of area and power for some loss in speed is quite acceptable in sub-10nm CMOS technologies, where power density and area gains are more valuable than frequency of switching.

The use of WFE approach for logic gate design is not limited to the standard two-input logic gate blocks, but can also be utilized to design multiple-input logic blocks for novel ultra-compact and low power circuitry in sub-10nm. In the following sections, this will be exemplified by a four-input NAND and four-input NOR gate.

III. 2T 4-Input NAND Gate

The first multi-input circuit we propose is a 2T four-input NAND gate consisting of a single p-like pull-up SBMOS FinFET and one n-like pull-down SBMOS FinFET. The pull up transistor is connected between the V_{DD} terminal and output node, the pull-down transistor is connected between output and the ground node as usual. The only difference between the pull-up and the pull-down transistor in this case is the gate work function values. It is found that the optimal switching is obtained when p-like SB FinFET has a work-function of 5.2 eV and the n-like SB FinFET has 4.2 eV for the gate metal work function. Both transistors have two independent-gate inputs all of which can be applied interchangeably to get a NAND function, making this design the extremely compact four input NAND gate. Both the circuit schematic and TCAD simulated logic function of the proposed four input NAND gate are shown in Fig.3. By the unique set of values chosen for the workfunction for the S/D contacts and the gates, the circuit is essentially a tug-of-war game between the transistors with unequal strengths. Only when the two inputs are high the p-like SB FinFET goes to OFF state, blocking the path between the V_{DD} and the output node. In the meantime, the high-threshold n-like SB FinFET turns fully ON completely discharging the output node to 0 logic level. In any other input combinations, as the p-like SB FinFET does not get fully turned OFF the

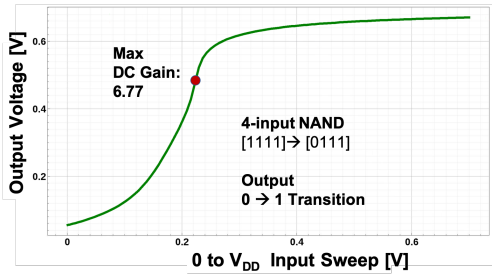

Fig. 4. DC sweep for 0 to 1 logic transition and gain analysis of the 4-input NAND circuit

TABLE I
PERFORMANCE OF THE 4-INPUT NAND BASED ON SB-FINFETS.

CMOS Static Logic Gate	Device Type	Stage/T Count	$\langle P \rangle$ [nW]	$\langle t_d \rangle$ [ps]	$\langle PDP \rangle$ [aJ]
NAND(A,B)	SB-FinFET	1stg / 2T	68.51	16.2	1.10
NAND(A,B)	FinFET	1stg / 4T	216.2	5.2	1.12
NAND(A,B,C,D)	SB-FinFET	1stg / 2T	141.4	54.3	7.68
NAND(A,B,C,D)	FinFET	2stg / 16T	774.4	23.6	18.25

output node gets high even if the NMOS transistor gets fully ON. This is mainly due to the much higher conductivity of p-like FinFET than n–like counterpart. Hence, by the help of convenient gate metal work functions, the ON and OFF state of the circuit gets selected by the state of p-like SB FinFET. The simulated logic output of Fig.3 not only confirms this behavior in all sixteen input states, it also discloses a minor ($< 20\,\text{mV}$) drop on logic outputs when each time n–like device is fully turned ON.

To further analyze and quantify the performance of logic transitions in the proposed 4-input NAND circuit, a DC sweep is also provided in Fig. 4 at the specific input states that lead to 0 to 1 transition. According the resulting data, the maximum DC gain during the transition is 6.7, which is adequate for the current design. This figure can be systematically analyzed for different values of the S/D barrier heights, gate dielectrics and semiconductor band-gaps in the design of the proposed circuits. A comparison of the switching power and delay of the proposed logic elements with the two and four-input conventional and SB-FinFET counterparts can be found in Table I. The data discloses a lower power-delay product for the 4-input ultra-compact SB-FinFET circuit by 42%. Power dissipation is significantly ($5\times$) lower for the 2T case since the one-stage logic gate is optimized to minimize parasitics and transistor count. The proposed four-input NAND circuit is $2.3\times$ slower than the conventional FinFET, because of its lower ON current, which is a characteristic of the SB-FinFETs also visible in the two input case also included in Table I. The slight loss at the output logic levels in Fig.3 that lead to static leakage did not cause a major performance degradation.

IV. 2T 4-INPUT NOR GATE

The second four-input circuit proposed in this work is the NOR circuit (see Fig.5a), which is essentially the polar opposite of the previous NAND circuit, from a functional point of view. However, the topology remains the same and the only change is actually in the workfunction values used: The p-like

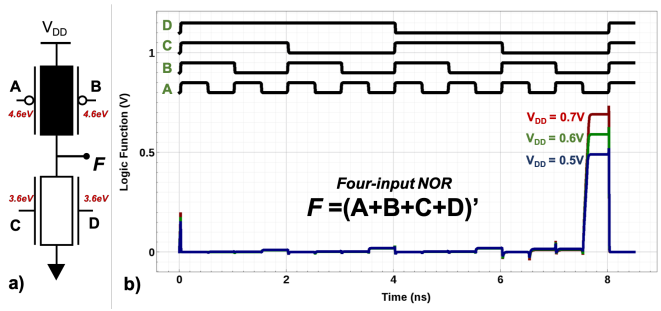

Fig. 5. a) Proposed ultra-compact (2T) four-input NOR circuit using SB-FinFETs employing WFE and b) the corresponding logic verification via TCAD simulations.

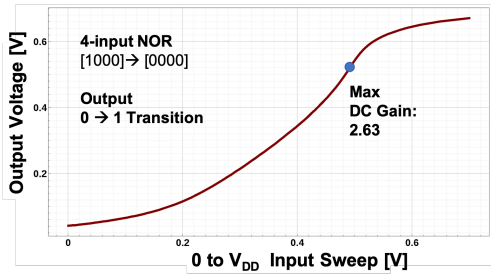

Fig. 6. DC sweep for 0 to 1 logic transition and gain analysis of the 4-input NOR circuit

ambipolar SB-FinFET uses 4.6eV versus 3.6eV for the n-like device. Clearly, the workfunctions are not simple band-gap complements of previous values. This is not surprising for two reasons: SB height for the S/D contacts in these circuits is 5.0 eV, in order to balance hole and electron tunneling currents as a result of large difference effective masses of holes ($m_h^* = 0.6$) in the valance and electrons ($m_e^* = 0.2$) in the conduction band. [11] The second difference is the n-like and p-like transistors do not have identical carrier density and electrostatics as a result of effective density of states and quantum corrections used in the TCAD model. Therefore, a unique set of workfunctions are needed for the four-input NOR circuit.

The transient TCAD simulation (Fig.5b) is once again used to verify the logic operation and extract the switching performance of the four-input NOR circuit. As before, the analysis of the switching performance is summarized in Table II. Much like the previous case, the proposed four-input NOR circuit has superior PDP as compared to the conventional FinFET. It has significantly lower ($4\times$) power dissipation and is slower by $2\times$. DC gain (max. 2.6) associated with the 0 to 1 transition in the NOR circuit is shown in Fig.6, indicating that the proposed workfunctions result in a sufficient margin for logic-levels and can drive subsequent inputs without any concern.

TABLE II
PERFORMANCE OF THE 4-INPUT NOR BASED ON SB-FINFETS.

CMOS Static Logic Gate	Device Type	Stage/T Count	$\langle P \rangle$ [nW]	$\langle t_d \rangle$ [ps]	$\langle PDP \rangle$ [aJ]
NOR(A,B)	SB-FinFET	1stg / 2T	90.7	16.0	1.45
NOR(A,B)	FinFET	1stg / 4T	305.0	5.5	1.68
NOR(A,B,C,D)	SB-FinFET	1stg / 2T	167.8	49.5	8.31
NOR(A,B,C,D)	FinFET	2stg / 16T	683.5	25.1	17.14

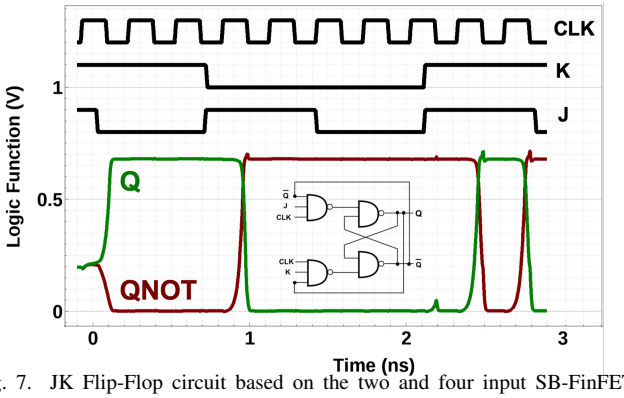

Fig. 7. JK Flip-Flop circuit based on the two and four input SB-FinFETs introduced above.

V. Application: 8T JK Flip Flop

In order to illustrate the significance of a compact and high performance multi-input logic gate, in this section, we provide a simple example based on a JK Flip-Flop. It is an important member of sequential logic blocks used in memory circuits and register files. It is basically a modified SR Latch to allow the forbidden state, when both inputs are high (i.e., S=1 & R=1), the output signal toggles. A JK Flip Flop has three different input signals which are J, K and CLK signals. Other than these signals to satisfy the aforementioned solution against the case for both inputs are high, two feedback lines are connected to one of the inputs of three-input NAND gates in the first stage. When J input becomes high while K is low the circuit does a "SET" operation (output going high). Opposite of this case (J=0 while K=1) is called the "RESET" state where output signal Q goes low.

Using the four-input NAND gate at its input stage, we can operate a compact and low-power JK Flip-Flop, as shown in Fig.7. In doing so, we reduce the overall logic pathway to two stages (as compared to two-input circuits) while also saving area and power associated with the extra gate at the input. The TCAD simulations verifies that J-K Flip-flop operates correctly. The same simulation data was also used to calculate the PDP figures in Table III that indicates that overall PDP figure for the SB-FinFET based compact version is lower by 5×. In this case the difference in the delay between the proposed 8T JK Flip-Flop and conventional 28T counterpart is much less, being only 20%. Also found in the previous tables introduced above, this has been a recurring theme in both logic gates and more complex digital blocks designed using the SB-FinFETs [8], [9]. It can be associated with the fact that SB-FinFETs offer significantly lower ON and OFF currents and conventional p/n junction FinFETs used in the 28T J-K Flip-Flop design have significantly higher speed even if they have more stages. Thus the real benefit of the proposed multi-input gates in complex and large circuits is their ability to lower area and power overheads, not the speed of switching.

VI. Conclusions

This work introduced, verified and analyzed the performance of ultra-compact 2T four-input NAND and NOR circuits based on 7nm SB-FinFETs via TCAD simulations. The approach uses work-function engineering of independent-gate Schottky-Barrier FinFETs that utilizes two carefully adjusted gate workfunctions as well as S/D contacts to accurately set individual device thresholds and injection of carriers to the ambipolar channels. Four-input NAND & NOR gates display similar advantages and challenges: They have lower (on average 45%) PDP figures, which is due to their substantially (as much as 5×) lower power dissipation in spite of their 2× longer switching times. The potential of the proposed NAND circuit to design ultra-compact and low-power logic circuits was verified via a case study for the J-K flip flop design.

TABLE III
Performance Comparison for JK Flip Flop Circuits based on four-input NAND with SB-FinFETs versus conventional design employing two-input NANDs with standard FinFET

CMOS Logic Gate	Device Type	Stage/T Count	$\langle P \rangle$ [nW]	$\langle t_d \rangle$ [ps]	$\langle PDP \rangle$ [aJ]
$FlipFlop(J,K)$	SB-FinFET	8T	244.8	46.25	11.32
$FlipFlop(J,K)$	FinFET	28T	1466.9	37.75	55.38

VII. Acknowledgements

This research was partially supported by NSF grants CCF-1513606, CCF-1703013 and CCF-1901192. TFC received financial support from the NQPI of Ohio University.

References

[1] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital integrated circuits*. Prentice hall Englewood Cliffs, 2002, vol. 2.
[2] A. De and S. Ghosh, "Threshold voltage defined multi-input complex gates," in *2017 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 2017, pp. 164–164.
[3] L. Qu, X. Cui, X. Xu, X. Cui, and Y. Ma, "The multi-input mrl logic gate and its application," in *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2019, pp. 1–2.
[4] K. Dubey, R. Marshal, and G. Lakshminarayanan, "Design of majority logic based comparator," in *2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT)*, 2018, pp. 1–6.
[5] A. Luck, S. Jung, R. Brederlow, R. Thewes, K. Goser, and W. Weber, "On the design robustness of threshold logic gates using multi-input floating gate mos transistors," *IEEE Transactions on Electron Devices*, vol. 47, no. 6, pp. 1231–1240, 2000.
[6] M. Kwon, H. Kim, J. Park, and B. Park, "Boolean logic circuit implementaion using multi-input floating-body mosfet," in *2015 Silicon Nanoelectronics Workshop (SNW)*, 2015, pp. 1–2.
[7] V. Beiu, J. M. Quintana, and M. J. Avedillo, "Vlsi implementations of threshold logic-a comprehensive survey," *IEEE Transactions on Neural Networks*, vol. 14, no. 5, pp. 1217–1243, 2003.
[8] T. F. Canan, S. Kaya, A. Karanth, H. Xin, and A. Louri, "Ambipolar sb-finfets: A new path to ultra-compact sub-10 nm logic circuits," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 255–263, 2018.
[9] T. F. Canan, S. Kaya, A. Karanth, and A. Louri, "Ultracompact and low-power logic circuits via workfunction engineering," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 5, no. 2, pp. 94–102, 2019.
[10] S. Pregl, A. Heinzig, L. Baraban, G. Cuniberti, T. Mikolajick, and W. M. Weber, "Printable parallel arrays of si nanowire schottky-barrier-fets with tunable polarity for complementary logic," *IEEE Transactions on Nanotechnology*, vol. 15, no. 3, pp. 549–556, May 2016.
[11] J. Guo and M. S. Lundstrom, "A computational study of thin-body, double-gate, schottky barrier mosfets," *IEEE Transactions on Electron Devices*, vol. 49, no. 11, pp. 1897–1902, Nov 2002.