Ambipolar SB-FinFETs: A New Path to Ultra-Compact Sub-10 nm Logic Circuits

Talha F. Canan, *Student Member, IEEE*, Savas Kaya, *Senior Member, IEEE*, Avinash Karanth, *Senior Member, IEEE*, Hao Xin, *Fellow, IEEE*, and Ahmed Louri, *Fellow, IEEE*

***Abstract*— Ultracompact sub-10-nm logic gates based on ambipolar characteristics of Schottky-barrier (SB) FinFETs and gate workfunction engineering (WFE) approach are introduced. Novel logic gate designs are proposed using WFE, whereby adjustment of workfunction in the contacts as well as two independently biased FinFET gates leads to an unprecedented degree of freedom for logic functionality that has not been explored before. The use of SB contacts, along with the high-k gate dielectric and ultrathin body, bestows a high-degree of short-channel immunity to the SB-FinFETs with ambipolar current–voltage characteristics down to 5 nm. The unique trait of the proposed novel logic gates is to lower CMOS transistor count by 50% and hence reduce overall area and power dissipation significantly. To illustrate this potential, an entirely novel conjugate (n/p channel) CMOS pass-gate transistor that can function as a two-transistor (2T) xor and minimalist 2T nand/nor gates is designed and verified with TCAD simulations. Depending on the gate designed, TCAD simulations indicate that judicious choice of gate workfunctions between 3.7 and 5.2 eV can lead to CMOS logic gates with a power–delay product (PDP) at 5×10^{-18} J level with immunity to ±0.1-eV workfunction variations. It is shown that WFE in independent-gate SB-FinFETs can lead to ultracompact logic circuits with 50% reduction in area and up to 10 times reduction in power, without significant degradation to overall PDP performance due to slower switching response compared with the conventional designs with p-n junction FinFET counterparts.**

***Index Terms*— Ambipolar, CMOS logic gates, nanotechnology, Schottky-barrier (SB) MOSFET, tunneling.**

Manuscript received September 8, 2018; revised September 26, 2018; accepted September 29, 2018. Date of publication October 31, 2018; date of current version December 24, 2018. This work was supported by the National Science Foundation under Grant CCF-1054339 (CAREER), Grant CCF-1420718, Grant CCF-1513606, Grant CCF-1703013, Grant CCF-1547034, Grant CCF-1547035, Grant CCF-1540736, and Grant CCF-1702980. The review of this paper was arranged by Editor M. M. Hussain. *(Corresponding author: Savas Kaya.)*

T. F. Canan, S. Kaya, and A. Karanth are with the School of Electrical Engineering and Computer Science, Ohio University, Athens, OH 45701 USA (e-mail: tc675716@ohio.edu; kaya@ohio.edu; kodi@ohio.edu).

H. Xin is with the Department of Electrical and Computer Engineering, The University of Arizona, Tucson, AZ 85721 USA (e-mail: hxin@ece.arizona.edu).

A. Louri is with the Department of Electrical and Computer Engineering, George Washington University, Washington, DC 20052 USA (e-mail: louri@gwu.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2874000

I. Introduction

AS THE last decade of downscaling of silicon CMOS devices in sub-10-nm scale is unfolding, options for viable, reliable, relatively simple Si MOSFET architectures that can deliver the required I_{ON}/I_{OFF} current ratios is rather limited. Hence, maintaining the course of gradual and minimalist changes to the current FinFET devices, as opposed to substantial changes to the material set or processing tools, still appears to be the most pragmatic approach [1]–[3]. Not only such minimalist approaches would provide additional time for a paradigm-shifting alternative to Si CMOS to be fully developed, but it would also present the least effort both financially and technologically. In this paper, we expand on our initial report [4] that introduced such an effort to extend conventional CMOS logic via gate workfunction engineering (WFE) [5]. We present a more accurate optimization that includes quantum corrections, a broader account of WFE approach to build ultracompact, relatively simple logic gates down to 5-nm scale, while also increasing the logic density by the way of independent-gate control in FinFETs. Assuming that accurate workfunction values can be set independently for n- and p-type FinFETs gates, we illustrate how ultrahigh density logic gates with a substantial reduction in total area and power dissipation can be implemented for sub-10-nm MOSFETs. Although such independent integration of two metal gates on narrow fins with a tight pitch would be challenging, we show that it could have substantial benefits for logic design, as exemplified in a 4-to-1 multiplexer (MUX) circuit.

The main premise of the proposed compact logic gates is the fact that an ambipolar device is capable of working both as a p- or n-type MOSFET that can be utilized in CMOS gates demanding equal current drive of both types [6]–[8]. When realized in the body of a single FinFET with two independent gates, then the ambipolar operation effectively translates to a single transistor pass gate that can operate with any combinations of two n- or p-type channels depending on the choice of gate workfunction. This leads to a unique XOR functionality out of only *two*-transistor (2T) FinFET cells [4], assuming that $\overline{A}$ and $\overline{B}$ are available. The WFE approach also allows for the redesign of low and high threshold FinFET devices key to the 2T NAND and NOR functionality that was originally proposed by IBM in 2006 using gate oxide and/or doping engineering [9], which is not feasible in

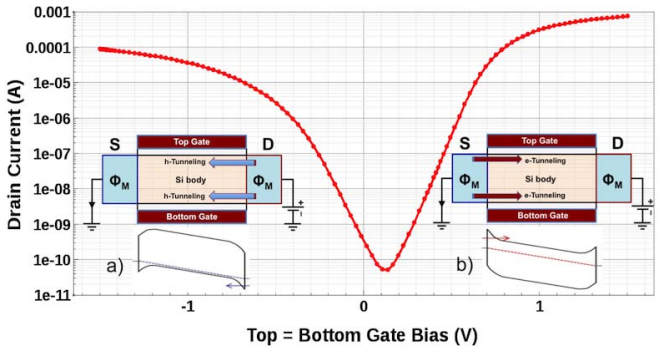


Fig. 1. I_D–V_{fg} characteristics of an ambipolar FinFET with midgap (4.6 eV) S/D contacts. Note the asymmetry in ON currents as well as minimum current. $L_g = 7$ nm, $t_{OX} = 1$ nm, $\epsilon_{OX} = 26$ (HfO_2), $t_{Si} = 4$ nm, and $V_{DS} = 0.5$ V.

sub-10-nm devices. In other words, the proposed WFE optimization may present a new route to explore competitive and dense logic performance in a sub-10-nm CMOS design.

Overall, it will be demonstrated that the proposed 2T XOR/NAND/NOR gates based on independent Schottky-barrier (SB)-FinFETs could lead to substantial gains in logic density, reduction of parasitics, novel logic gates (1T CMOS pass gate), low power consumption (OFF current), and good potential for scaling down to 5 nm and for low-supply (0.6 V) operation. While a standard silicon FinFET device is used to validate the WFE approach for industrial and practical reasons, it should be pointed out at the outset that other ambipolar devices, such as 2-D crystals [10], III–V semiconductors [11], or carbon nanotube (CNT) channels [8], [12], where an independent pair of bottom and top gates can be created, can also be used to implement transistor architectures presented here. Thus, the proposed WFE approach is relevant for both practical industrial Si FinFETs and for any device that possess ambipolar current–voltage (I–V) characteristics.

II. SB-FinFET Device Simulation

The main device element enabling the WFE approach is the SB FinFET (Fig. 1) that employs metallic (typically silicided) source and drain contacts instead of slower and space-charge prone p-n junctions that have become especially problematic as gate dimensions are scaled to 10 nm [13]. This generic ambipolar FinFET transistor ($t_{ox} = 1$ nm, $\epsilon_{ox} = 12$, and $t_{Si} = 4$ nm) with metallic SB source/drain (S/D) contacts is capable of ambipolar carrier injection [13], [14] and can address many issues, such as poor subthreshold slope, larger capacitive parasitics, dopant fluctuations, as well as incompatibility with novel 1-D/2-D channel materials (e.g., nanowires, CNT, or graphene). The type of tunneling carriers (i.e., the silicide barrier height), rather than the heavy doping in a p-n junction, determines the characteristics of an ambipolar SB-FinFET, as indicated in Fig. 1. Typically, p-type devices have larger than midgap (~4.6 eV for Si) workfunctions for S/D contact so as to lower the barrier height for holes and vice versa for electrons. The major drawback for SB-FinFETs is the additional series resistance associated with tunneling and reduced ON current. As a result, at longer gate lengths, SB FinFETs could not quite compete with dominant p-/n-junction FinFET switches in a conventional logic performance [14], [15]. However, this situation can reverse in sub-10-nm operation: OFF current also reduces due to the tunneling barrier and the overall I_{ON}/I_{OFF} ratio in SB-MOSFETs becomes acceptable for logic operation. In fact, lower I_{ON} is especially welcomed for reduced heating, which offers a major advantage over conventional devices.

Our initial analysis on the use of WFE for logic gates has utilized a simplistic drift-diffusion (DD) model for the TCAD simulations for a proof-of-concept study [4] In this paper, we provide a much more detailed simulation analysis based on the first-order quantum mechanical corrections via density-gradient approach that is necessary to accurately select gate workfunctions fundamental to the type of logic operation. Given the device dimensions, carrier quantization and ensuing modification to the channel and barrier potentials must be accounted for accurate device design, which can be achieved to a large degree using density-gradient corrections implemented in the TCAD suite [16]. Carrier injection through S/D contacts is modeled using the energy-dependent barrier tunneling model in the TCAD, which utilizes the Wentzel–Kramer–Brillouin model to calculate tunneling rates. In this paper, we also explore a broader range of workfunctions, update dimensions FinFET ($L/t_{Si} = 10/7$, 7/4, or 5/3 nm) in better conformity with the published literature [1]. Hence, this paper constitutes a more accurate and broad account of a WFE-based logic gate design.

Another design consideration is the choice of effective masses for the electron (m_e^*) and hole (m_h^*) injection through the S/D contact barriers. Since the barrier high is a design parameter, we did not make *a priori* assumption as to which silicide material (SB height) and effective mass should be chosen for the optimization study. Moreover, the exact nature of interface (chemical uniformity and atomic sharpness) between the Si channel and silicided contacts would also impact the values for m_e^* or m_h^*, which can complicate the effective mass choice further. However, due to quantum mechanical (QM) quantization, lower transverse effective mass of silicon X-valleys and lighter holes is more commonly preferred [7], [11]. Due to higher hole mobility along the [011] direction, there is additional pretext for the use of lighter hole mass. In fact, the choice of m^* does *not* dramatically alter the simulated I–V characteristics of SB-FinFETs within the practical range of values reported in the literature, as can be seen in Fig. 2 that compares different sets of effective mass values. Accordingly, we assume $m_e^* = 0.2$ and $m_h^* = 0.6$ for the rest of this paper.

III. 1T Ambipolar Pass Gate and 2T XOR

The presence of Schottky S/D contacts in FinFETs lifts up the potential at either end of the channel that would otherwise slip away from gate control due to depletion region of p-/n-junctions in the conventional design, thus improving device scalability. However, the two gates are physically one structure in standard FinFETs and driven together for a maximum logic performance (I_{ON}/I_{OFF} ratio). This would create sufficiently thin and low barriers to tunnel only for one

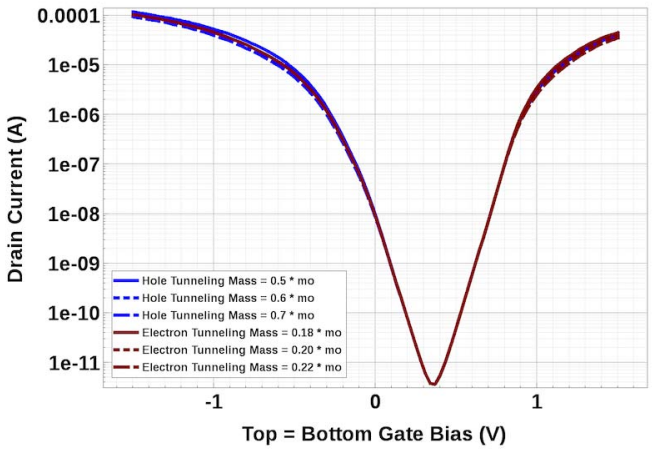


Fig. 2. Choice of tunneling effective mass for electrons and holes does not dramatically alter the ambipolar SB-FinFET *I–V* characteristics. Nominal case for simulation is $m_e^* = 0.2$ and $m_h^* = 0.6$. Workfunction for TG/BG is assumed to be midgap (4.6 eV) and S/D contact to be 5.0 eV.

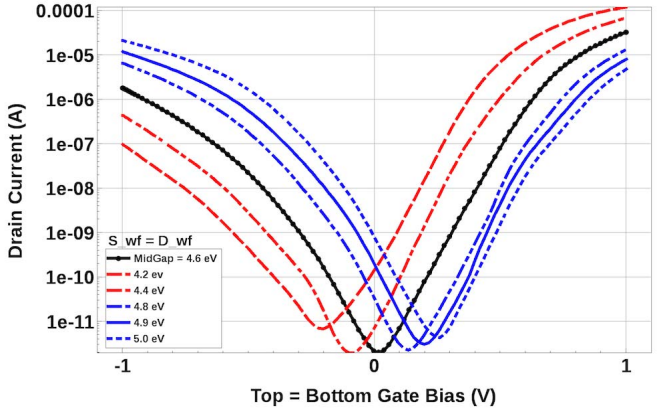


Fig. 4. Balanced ambipolar currents at $V_{DS} = 0.5$ V is only possible for S/D workfunction of ~4.9 eV, i.e., reduction (increase) of hole (electron) barrier, resulting in depletion mode $V_{tp} > 0$ for hole channels and $\min(I_D) =\sim 0.3$ V. Workfunction for TG/BG is assumed to be midgap (4.6 eV).

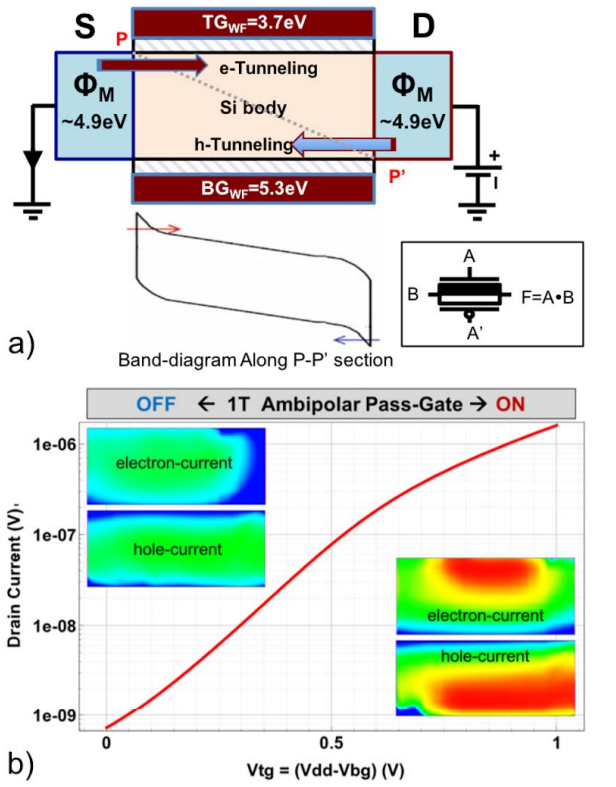


Fig. 3. Proposed SB-FinFET with parameters optimized for conjugate dual channels. (a) Bottom gate for hole tunneling/conduction and top gate for electron tunneling/conduction. (b) Simulated characteristics of the optimized 7-nm ambipolar pass gate and the corresponding e/h current densities in ON and OFF cases (insets) for $V_{ds} = 1.0$ V bias.

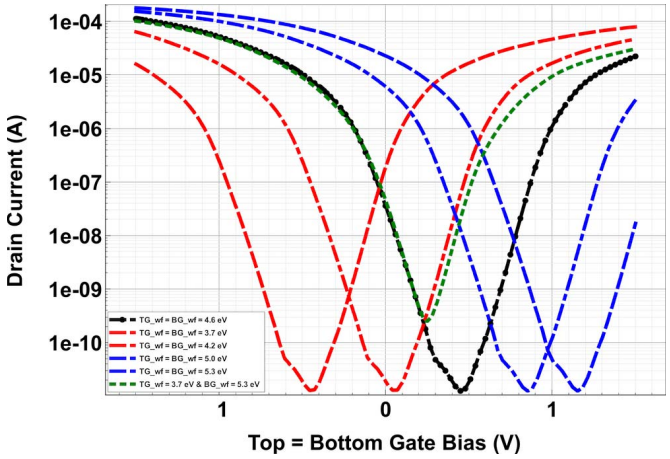


Fig. 5. Setting top and bottom gate workfunctions to near band edge values (3.7 and 5.3 eV) can provide an inherent "electrostatic bias" in top and bottom channels for hole and electron injection, respectively, akin to a CMOS pass gate.

end of the channel and one type of carrier (see Fig. 1). Thus, the inherent "duality" of the channels cannot be exploited in the same body, and the device can only function as *either* an n-type *or* p-type FinFET at a given gate bias. However, if and when the FinFET gates are built from *two* different metals (possible by a few additional steps on the current FinFET process [17], [18]), this duality can be exploited at two separate channels under *each* gate, as shown in Fig. 3.

This novel configuration is analogous to pass-gate (or transmission-gate) CMOS pair with parallel n-/p-type MOSFETs driven with opposing logic states. For the optimized 7-nm SB-FinFET in this figure, two distinct ambipolar channels in a single body, associated with unique gate workfunctions chosen, can be clearly seen, with three orders of magnitude change in device resistance between ON/OFF states. Hence, using WFE, we can build a 1T CMOS ambipolar pass-gate device with two independently driven gates, which can be utilized to construct very compact CMOS circuits.

Having shown that a 1T pass-gate functionality is present in an ambipolar SB-FinFET with independent gate drive, it is necessary to provide a clear strategy to show how to attain and optimize this conjugate channel operation for logic performance. This is accomplished in Figs. 4 and 5 using the same generic device structure. In the design process, first, S/D workfunction is substantially shifted toward valance band (~4.90 eV) in order to obtain similar ON currents for two channels. This is compulsory as a large difference

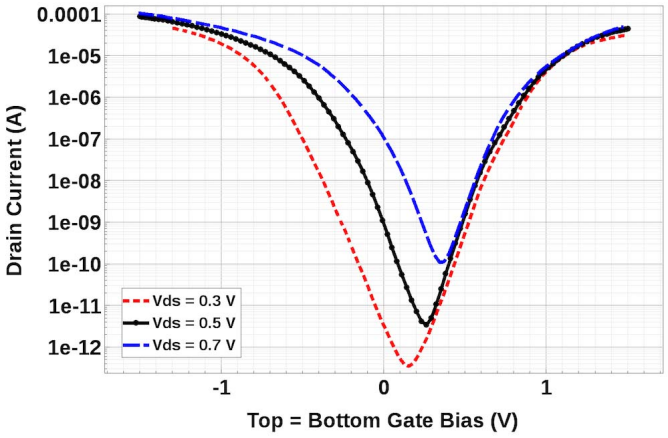


Fig. 6. Impact of drain bias on optimized 1T ambipolar pass gate.

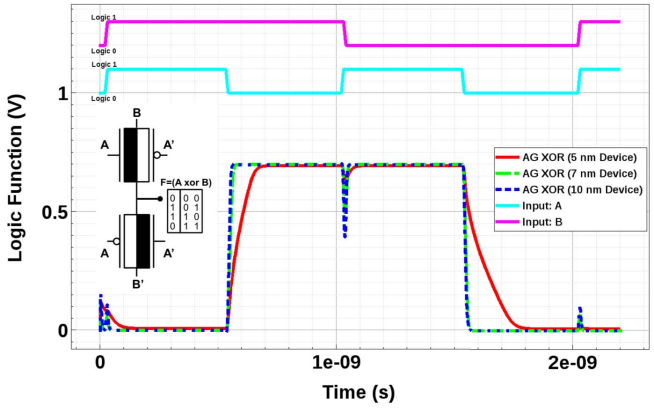


Fig. 7. Verification of ambipolar 2T xor functions via TCAD simulation down to 5-nm gate length for a supply voltage of 0.7 V.

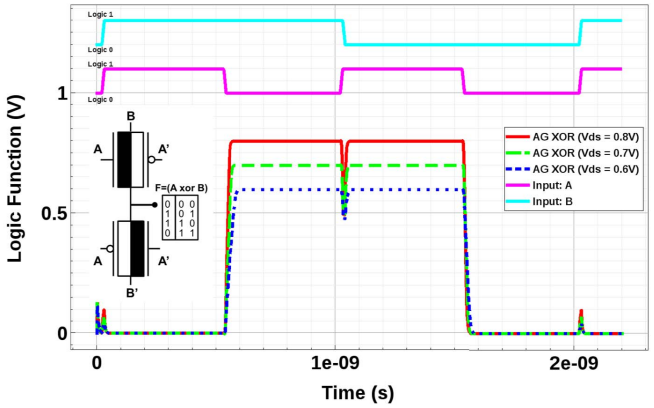


Fig. 8. Simulated 2T xor functions of 7-nm ambipolar FinFETs for the V_{dd} values of 0.8, 0.7, and 0.6 V

between electrons and holes in terms of effective masses for quantization, tunneling ($m_e^* = 0.2$ and $m_h^* = 0.6$), and density of states can result in up to two orders of magnitude difference in ON currents. In other words, the visibly uneven ambipolar behavior resulting from the use of equal midgap workfunctions (4.6 eV) in Fig. 1 necessitates lowering (raising) barriers for holes (electrons). Fig. 4 shows that S/D contact workfunction 4.9 eV gives almost equal n/p channel currents for a drain bias of 0.5 V. Next, the top and bottom gates can be "electrostatically" biased (thresholds lowered) for the injection of either type of carriers by the choice of opposing workfunctions (3.7 versus 5.3 eV), as shown in Fig. 5, which illustrates the significance of setting *different* and *opposite* gate workfunctions to alter branch currents in one-transistor (1T) pass-gate operation. Although the use of unequal workfunctions would place additional demands on device fabrication, they are well within a current level of gate engineering (epitaxial growth or atomic layer deposition/chemical vapor deposition processes) [9], [15]. It is worth pointing out that ambipolar pass gate is still vulnerable to significant changes in the tunneling current due to drain-bias-induced changes (depletion effects) to the SBs at the S/D contacts, which can upset the balanced ambipolar behavior. Although $V_{DS} = V_{DD}/2 = \sim 0.5$ V is chosen for Figs. 4 and 5, this value may not be necessarily the best choice for a given logic switching performance at full V_{DD} bias. To illustrate the impact of dynamic drain bias on the optimal I–V curves, Fig. 6 includes the simulated characteristic of the "1T pass-gate" device (3.7 versus 5.3 eV) for three different V_{DS} biases. Clearly, drain bias effects the hole tunneling current more readily, especially in the OFF-current levels. Thus, during the XOR logic switching, the assumption of *static* V_{DS} bias of 0.5 V can lead to suboptimal performance, having much lower hole currents initially then assumed. In fact, our subsequent simulation analysis indicates that more optimal logic gates typically require the S/D workfunctions of $\phi_B = 5.0$ eV, increasing the hole current slightly.

Following the above-mentioned procedure, two of the optimally designed 7-nm ambipolar pass gates can be used to operate as an XOR gate, as shown in Fig. 7. The XOR logic switching is correct and transitions are symmetrical for $L = 7$ nm case. In fact, the same optimization is valid also for the $L = 10$ nm ($t_{Si} = 7$ nm) and $L = 5$ nm ($t_{Si} = 3$ nm) XOR gates. The 5 nm case is clearly showing the signs of slower switching due to higher thresholds resulting from quantum mechanical discretization. Such a performance loss can be compensated by adjusting the optimal workfunctions specifically for the 5-nm device. The middle glitches in these logic plots are due to relatively slow input rise/fall times adapted to guarantee convergence. Moreover, the 7-nm ambipolar XOR operates equally well under different supply voltages when $0.6 \leq V_{DD} \leq 0.8$ V (see Fig. 8). Hence, optimization holds for a wide range of device dimensions and operating conditions. Both logic device concepts (1T pass gate and 2T XOR) can be utilized to dramatically reduce transistor counts and device area for a wide variety of logic functions where pass gates are preferred, such as full adders and MUXs.

Testimony to the proposed optimization approach mentioned earlier is Fig. 9, which shows that ambipolar XOR gate properly switches as the TG/BG workfunctions shift toward the band edges. For $TG_{WF} > 4.0$ eV and $BG_{WF} < 5.1$ eV, performance of the XOR gate quickly deteriorates, completely malfunctioning for workfunction values near the midgap value (4.6 eV).

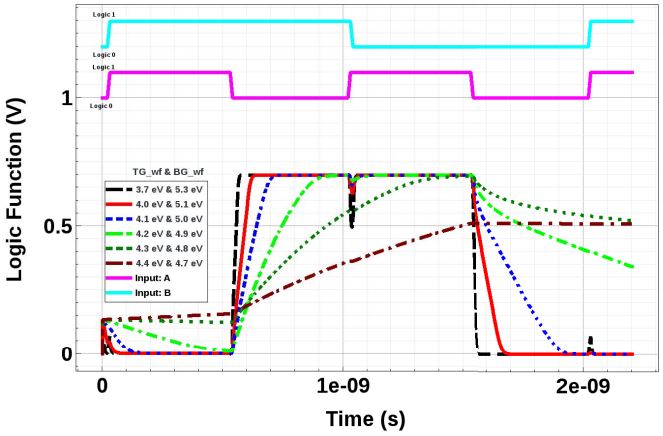


Fig. 9. Demonstration of the optimal workfunction for the 2T xor gate. As the used workfunctions approach to the midgap value (4.6 eV), the conjugate electron and hole channels loose distinct behavior and xor operation fails. For S/D contacts, $\phi_B = 5.0$ eV.

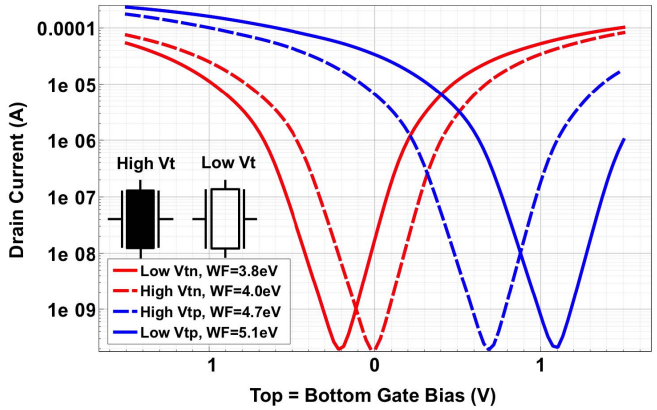


Fig. 10. *I–V* characteristics of ambipolar FinFETs optimized for low and high threshold FinfETs of both polarity. WF for S/D is 5.0 eV and TG = BG as given in the legend.

IV. 2T NOR and NAND via Ambipolar FinFETs

Chiang *et al.* [19] and Zhang *et al.* [20] have already shown by simulation that a single high-V_{tn} independent gate FinFET can be utilized as an AND logic pull-down element that only conducts if both gates are biased with logic 1 (V_{DD}) input. This creates an extremely compact 2T NAND gate that has been shown to reduce both power (40%) and delay (10%), culminating in an absolutely minimal logic gate arrangement. A similar arrangement can be made for p-MOS pull-up network in CMOS NOR gates, replacing two series pMOS with a single independent-gate high-V_{tp} SB-FinFET. However, the original work suggested using *oxide thickness* to adjust for high-V_t, which is impractical and suboptimal for sub-10-nm devices that would suffer from the high subthreshold slope. In our approach, as shown in Fig. 10, using the *I–V* characteristics optimized only by the choice of gate workfunctions, it is possible to implement high and low threshold variants of the n- or p-type SB-FinFETs, which can be used to build 2T NAND/NOR gates.

According to the logic operations in Figs. 11 and 12, only a pair of ambipolar SB-FinFETs with low-V_{tp} (empty FinFET symbol) and high-V_{tn} devices (filled symbol) in series arrangement will work as a NAND logic gate. Similarly, in the opposite arrangement, a NOR logic operation is also confirmed. Moreover, in all cases, the logic gates are found to operate correctly with supply voltages as low as 0.6 V and gate lengths as short as 5 nm using this exact same arrangement of workfunctions. In other words, the proposed workfunction optimization is relevant and practical for all ranges of 2T NAND/NOR gates and operating conditions explored. Thus, together with the use of 2T-XOR gates, WFE can lead to ultracompact logic circuits that have never been explored before. Of course, the main challenge of these high and low threshold devices is the introduction of new gate electrode metals (or silicides) with the correct workfunction, which is not trivial but possible as will be discussed next.

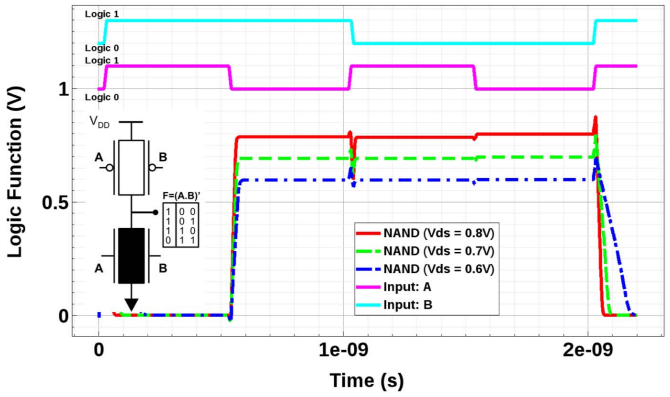


Fig. 11. Verification of ambipolar 2T nand function via TCAD simulation. nand operation is confirmed with supply voltages as low as 0.6 V using the same optimized workfunctions

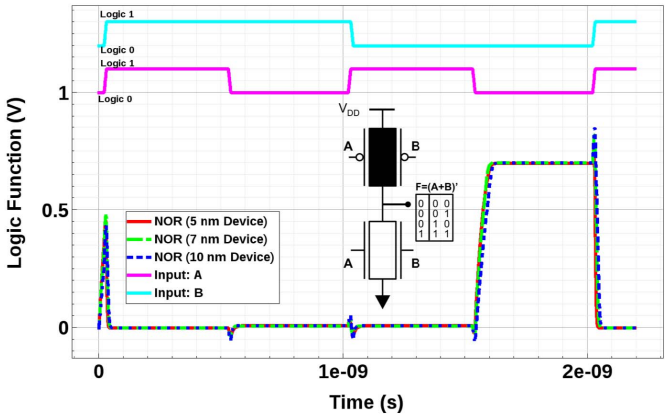


Fig. 12. Verification of ambipolar 2T nor function via TCAD simulation. nor operation is confirmed down to 5-nm gate length using the same optimized workfunctions

V. Performance Analysis

In this section, a brief evaluation of the performance of the proposed logic gates is provided, including dynamic performance, power dissipation, tolerance for process variability, and gate area. These important figures of merit for logic performance are summarized in Table I for both ambipolar gates proposed and conventional FinFET counterparts.

TABLE I
STATISTICAL STUDY OF PERFORMANCE FOR 7-nm WORKFUNCTION ENGINEERED 2T LOGIC GATES BASED ON AMBIPOLAR SB FinFETs. *2T INVERTERS WERE NOT INCLUDED IN PDP AND AREA CALCULATIONS FOR XORS

Logic Gate	S/D Φ_m [eV]	P_{gate} Φ_m [eV]	N_{gate} Φ_m [eV]	$< P >$ [nW]	$< t_d >$ [ps]	$< PDP >$ [aJ]	σ_{PDP} [aJ] (%)	$\pm 0.1eV$ Yield [%]	Area [λ^2]
2T Ambipolar NOR	5.0	4.7	3.8	8.96	36.1	4.25	0.86 (20.2%)	100	165
2T Ambipolar NAND	5.0	5.1	4.0	8.41	52.2	5.41	1.86 (34.3%)	81.4	165
2T Ambipolar XOR*	5.0	5.3	3.7	78.0	21.1	1.57	0.38 (24.2%)	100	132
4T Standard NOR	4.6	4.6	4.6	16.4	5.15	2.44	0.48 (19.7%)	100	231
4T Standard NAND	4.6	4.6	4.6	26.6	4.39	1.48	0.12 (08.1%)	100	231
4T Standard XOR*	4.6	4.6	4.6	958	6.62	3.77	0.21 (05.6%)	100	260

The gate workfunctions in each posted device correspond to the optimal values of TG&BG WF for XOR (5.3 and 3.7 eV), NAND (5.1 and 4.0 eV), and NOR (4.7 and 3.8 eV) as concluded from the earlier optimization explained. For conventional devices, gates were assumed to be the same metal with a midgap value (4.6 eV). In all cases, 7-nm devices with $W/L = 11$ are used to construct this table for brevity, but similar observations are also made for other gate lengths explored. To provide a fair comparison, the table also includes "control" devices in the form of standard 4T logic gates employing conventional p-/n-junction FinFETs (no SB S/D) with midgap metal (4.6 eV) on both gates driven symmetrically. Hence, these "control" designs will require twice the number of transistors, but they would also set an *upper limit* for performance as they have symmetrical gate drive that leads to more than doubling of transconductance (g_m). Moreover, in order to probe the resilience of the proposed gates against the process variability in setting the optimal workfunctions, we also carried out of 27 simulations for each logic function at process corners (± 0.1 eV variations in S/D, TG, and BG barrier heights) results of which are utilized for the statistical assessments. The most essential figure of merit for logic gates is the power–delay product (PDP), an integral measure of switching delay and power dissipation. Average $\langle$PDP$\rangle$ of the proposed 7-nm ambipolar gates for $V_{DD} = 0.7$ V is found to be 4.25×10^{-18}, 5.41×10^{-18}, and 1.57×10^{-18} J for NOR, NAND, and XOR gates, respectively. While these values are not accurate given the finite parasitics included in the TCAD model ($R_{S,D} = 10\ \Omega$ and $C_L = 1$ fF) and lack of gate tunneling (i.e., static leakage) in the present simulations, they do indicate a very competitive logic performance for the proposed circuits compared with the standard 4T logic gates. In fact, the 2T ambipolar XOR outperforms 4T conventional counterparts even in terms of average PDP, presumably due to lower overall parasitics, even though they do have more variability as evident from the standard deviation of PDP (σ_{PDP}). Since tunneling though S/D SB is the defining feature on ambipolar FinFETs, higher sensitivity to workfunction variability is to be expected. The resulting standard deviations are typically $\leq$ 30% for ambipolar cases, with the NAND gates being the worst (34.3%). Moreover, according to the same table, a small subset of (19% of) NAND gates has displayed logic failure due to ± 0.1 eV variations to the barrier heights. All failure cases were associated with S/D contacts being set to 5.1 eV. Since all ambipolar NOR and XOR gates are worked under similar constraints, we believe that

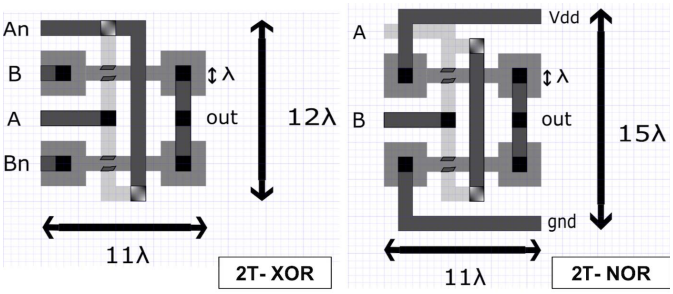


Fig. 13. Example layouts for the proposed 2T xor and nor circuits with independent-gate SB-FinFETs.

the failing NAND gates indicate that the adapted top (front) and bottom (back) gate workfunction values are suboptimal for NAND case. By adjusting the proposed WF values only slightly, the few failing NAND gates should be able to operate within typical error margins. Therefore, the WFE devices appear to be sufficiently robust for typical process variations in the metal workfunctions of $\pm 0.1\ eV$. In any case, a separate set of WF values may always be available for gates if S/D workfunction is readjusted, following the design principles introduced in the previous sections. In addition, a general assessment of area for the ambipolar XOR, NAND, and NOR gates has also been undertaken based on the recent work of Kim *et al.* [21] and taking into account additional area to route independent-gate signals. This preliminary analysis shows that compact 2T gates can be laid out within $132\lambda^2$ and $165\lambda^2$ for XOR and NAND/NOR logic, respectively, where λ is the pitch for the Si channel as shown in Fig. 13. Compared to 4T conventional counterparts with symmetrically driven FinFETs that occupy 231 or 260 λ^2, the proposed 2T implementations offer $\sim$30% or $\sim$50% reduction in area for the NAND/NOR or XOR gates, respectively. However, lately, Intel offered a novel gate contact approach (contact on active gate) [22], [23], which can eliminate overheads associated with routing of independent gates altogether. Therefore, it should be possible to reach, or even slightly exceed, 50% area savings also for the 2T ambipolar NAND/NOR logic gates in sub-10-nm logic systems.

VI. DISCUSSION

It is necessary and fair to point out that the proposed device concept heavily relies on the capability of building independent gates of FinFETs with three or four

specific workfunctions. Due to the asymmetry of the electron and hole tunneling rates, these workfunctions are not symmetrical around midgap either. Moreover, the unequal impact of drain-bias-induced effects at full supply (see color density maps in Fig. 3) also contributes to the asymmetry of these optimal workfunctions. As the tunneling rates for channel carriers to and from S/D contacts is very sensitive to the barrier height, drain-induced barrier lowering effect indeed becomes somehow more of a challenge in SB-FinFET device optimization. For this reason, we set S/D workfunction $\phi_B =\sim 5.0$ eV in all the above-mentioned gates, which is slightly higher than the seemingly optimal I–V characteristics observed for $\Phi_{m,S/D} = 4.9$ eV optimized for $V_{\rm DD} = 0.5$ V case.

It is obvious from Table I, raw I–V curves and logic transients in the earlier sections, that the PDP improvements in the ambipolar 2T logic circuits are predominantly due to the ultralow power levels of the SB-FinFETs as opposed to its switching (20–50 ps) performance that lags behind the p-/n-junction counterparts. Introduction of tunneling barriers at the S/D contacts dramatically lowers OFF currents to 10 pA levels (see Figs. 2 and 5), along with a considerable drop in the ON-current levels (μA) that limits the logic switching speed. Since SB-FinFETs have a superior subthreshold slope (80–100 mV/decade) compared with conventional FinFETs in sub-10-nm scale, it is possible to lower the OFF current substantially. This implies that the WFE approach delivers essentially ultralow power (nW) logic circuits with 10-ps switching speeds on silicon in a sub-10-nm regime. Moreover, if applied to other material systems with channels that have considerably lower effective mass such as graphene, CNTs, or III–V semiconductors, the WFE approach could also offer an advantage in terms of speed. Both observations imply that WFE could be considered as a novel methodology for device design and optimization in the remaining years of downscaling.

Compared with our preliminary work on the WFE via DD-based simulations [4], the incorporation of the first-order quantum corrections via density-gradient approximation indicates that QM is essential for accurate design and optimization of the proposed circuits. Although the gate tunneling effect is still absent, the low-supply voltages used here should ensure that it will not seriously alter any of our conclusions in the following. Any adverse effect would be on the OFF current, which is extremely low and would not impact dynamic performance figures extracted.

While an introduction of three optimal workfunctions in different gates is indeed a real challenge in manufacturing, it is within the reach of current metal-gate CMOS processes and is easier than integrating entirely new channels or new device architectures, especially in the short term. In this regard, it is also helpful to note that there are other recent efforts [24], which explore the gate-function tuning for the independent FinFET for SRAM memory cells, which should give us additional confidence in pursuing the presented optimization and novel gate architectures for logic applications. Moreover, based on the demonstrated potential of WFE approach for logic design here, it is quite reasonable to develop this approach further and apply it to "cell-level" design. In this new design paradigm, WFE can be applied to the whole functional cell, such as a full-adder, MUX, or SRAM by adjusting/allocating multiple workfunctions to *specific* transistors rather than *every* transistor to optimize the cell function and performance. This novel approach has already produced very exciting results, which will be reported in a separate submission, as a sequel to this paper.

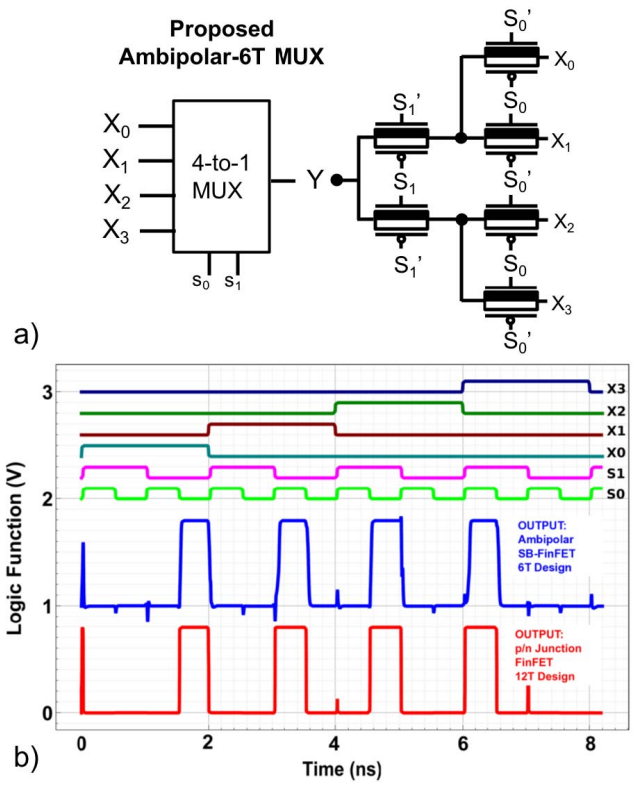


Fig. 14. Demonstration of 4-to-1 MUX circuits (a) using six ambipolar SB-FinFETs and (b) its logic response compared with conventional pass gates built via twelve p-n junction FinFETs.

VII. Application Example: 4-to-1 MUX

Potential of the proposed novel ambipolar XOR gate for compact and high-performance logic can be assessed via a simple 4-to-1 MUX circuit built using only three XOR pass gates (6T), as opposed to six pass gates (12T) in the conventional FinFET implementation, excluding the inverters for the select bits. Fig. 14 shows the topology of such a MUX circuit as well as its logic response obtained by the application of full 16-bit input combinations to 7-nm transistors for a $V_{\rm DD}$ bias of 0.8 V. The MUX circuit operates correctly for all input conditions. The same is true also with 5- and 10-nm versions (not shown). For comparison, the corresponding output for the conventional CMOS pass-gate design, employing six pairs of p-n-junction FinFETs, is also provided in Fig. 14(b). The dynamic performance of both the logic circuits extracted from these plots via MATLAB postprocessing is provided in Table II. The ambipolar version is clearly slower, by an order of magnitude. However, it consumes 5 times less power and 50% less area. Thus, the resulting PDP is ~40% larger for the ambipolar circuit. It must be pointed out that the delays from the MUX are an average of the 4 transitions in Fig. 14, while

TABLE II
SWITCHING PERFORMANCE OF THE PROPOSED ULTRACOMPACT 4-TO-1 MUX BASED ON 7-nm AMBIPOLAR SB-FinFETs COMPARED WITH THE CONVENTIONAL CMOS PASS-GATE DESIGNS WITH 12 TRANSISTORS. INVERTER DELAYS AND POWER ARE NOT INCLUDED

Pass-Gate Type in 4-to-1 MUX	$< P >$ [μW]	$< t_d >$ [ps]	$< PDP >$ [aJ]	NM Loss [mV]	Area [λ^2]
Ambipolar – 6*T*	10.42	38.25	398	∼10	442
CMOS – 12*T*	52.46	4.75	249	∼5	846

in Table I they were calculated from an ensemble of 27 simulations of varying workfunctions in a single XOR gate. Thus, they naturally differ. Yet, the general conclusion in both cases remains the same. The main advantage of the ambipolar gates is its *lower power consumption and area*, as opposed to their speed. This is actually an acceptable outcome, since modern decanano CMOS logic circuits, dominated by interconnection overheads, is limited only by power dissipation and not by switching speed. Given that the device downscaling is its final decade, the 50% reduction in area and 5 to 10 times lower power should present sufficient advantage for the ambipolar SB-FinFET circuitry to be considered for logic applications in the years to come.

VIII. CONCLUSION

A novel approach, contact and/or gate WFE, to design and operate ultracompact CMOS XOR, NAND, and NOR gates in sub-10 nm was proposed and verified via TCAD simulations. WFE is applied to independent-gate SB ambipolar FinFETs with specific gate workfunctions and can lead to unique logic circuits. In particular, we show how a single transistor CMOS pass-gate, with one pair of source–drain contacts and two opposite (n and p) types of channels, can be built using unequal gate workfunctions in an independent FinFET gate. Based on the 1T pass gate, we also illustrate how it is possible to design a minimalist 2T XOR gate. Similarly, novel 2T NAND and NOR gates have also been proposed using high/low threshold devices, utilizing two different workfunctions for the n- and p-type SB-FinFETs. Functionality of 2T logic gates has been confirmed via standard Synopsys TCAD tools that take into account band-to-band tunneling, barrier tunneling, as well as first-order quantum-mechanical correction via density-gradient approach. Dynamic performance and area of the 2T ambipolar gates are compared with the 4T conventional counterparts built using FinFETs with p-/n-junction contacts. It is found that ambipolar gates offer a reduction in the total area up to 50%, have competitive PDP at 1–5 $\times$ 10^{-18}J scale and are resilient to 0.1-eV fluctuations in the workfunction values. The proposed gates can be used to build extremely compact sub-10-nm logic gates that have especially low power dissipation, which was demonstrated via a 4-to-1 MUX application example.

REFERENCES

[1] T. Chiarella *et al.*, "Towards high performance sub-10 nm finW bulk FinFET technology," in *Proc. 46th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2016, pp. 131–134, doi: 10.1109/ESSDERC.2016.7599605.

[2] T. N. Theis and H.-S. P. Wong, "The end of Moore's law: A new beginning for information technology," *Comput. Sci. Eng.*, vol. 19, no. 2, pp. 41–50, Mar./Apr. 2017, doi: 10.1109/MCSE.2017.29.

[3] J. Koomey and S. Naffziger, "Moore's law might be slowing down, but not energy efficiency," *IEEE Spectr.*, Mar. 2015. [Online]. Available: https://spectrum.ieee.org/computing/hardware/moores-law-might-be-slowing-down-but-notenergy-efficiency

[4] T. F. Canan, S. Kaya, A. Kodi, H. Xin, and A. Louri, "Ultra-compact sub-10 nm logic circuits based on ambipolar SB-FinFETs," in *Proc. IEEE 60th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2017, pp. 100–103, doi: 10.1109/MWSCAS.2017.8052870.

[5] B. H. Lee, J. Oh, H. H. Tseng, R. Jammy, and H. Huff, "Gate stack technology for nanoscale devices," *Materialstoday*, vol. 9, no. 6, pp. 32–40, 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1369702106715413, doi: 10.1016/S1369-7021(06)71541-3.

[6] S. Pregl, A. Heinzig, L. Baraban, G. Cuniberti, T. Mikolajick, and W. M. Weber, "Printable parallel arrays of Si nanowire schottky-barrier-FETs with tunable polarity for complementary logic," *IEEE Trans. Nanotechnol.*, vol. 15, no. 3, pp. 549–556, May 2016, doi: 10.1109/TNANO.2016.2542525.

[7] J. Guo and M. S. Lundstrom, "A computational study of thin-body, double-gate, Schottky barrier MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 1897–1902, Nov. 2002, doi: 10.1109/TED.2002.804696.

[8] M. H. Ben-Jamaa, K. Mohanram, and G. De Micheli, "An efficient gate library for ambipolar CNTFET logic," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 30, no. 2, pp. 242–255, Feb. 2011, doi: 10.1109/TCAD.2010.2085250.

[9] M.-H. Chiang, K. Kim, C. Tretz, and C.-T. Chuang, "Novel high-density low-power logic circuit techniques using DG devices," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2339–2342, Oct. 2005, doi: 10.1109/TED.2005.856191.

[10] A. Prakash, H. Ilatikhameneh, P. Wu, and J. Appenzeller, "Understanding contact gating in Schottky barrier transistors from 2D channels," *Sci. Rep.*, vol. 7, no. 1, 2017, Art. no. 12596. [Online]. Available: https://www.nature.com/articles/s41598-017-12816-3, doi: 10.1038/s41598-017-12816-3.

[11] M. Schwarz, L. E. Calvet, J. P. Snyder, T. Krauss, U. Schwalke, and A. Kloes, "On the physical behavior of cryogenic IV and III–V Schottky barrier MOSFET devices," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3808–3815, Sep. 2017, doi: 10.1109/TED.2017.2726899.

[12] C. Qiu, Z. Zhang, M. Xiao, Y. Yang, D. Zhong, and L.-M. Peng, "Scaling carbon nanotube complementary transistors to 5-nm gate lengths," *Science*, vol. 355, no. 6322, pp. 271–276, Jan. 2017. [Online]. Available: http://science.sciencemag.org/content/355/6322/271, doi: 10.1126/science.aaj1628.

[13] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1048–1058, May 2006, doi: 10.1109/TED.2006.871842.

[14] Q. Huang *et al.*, "Self-depleted T-gate Schottky barrier tunneling FET with low average subthreshold slope and high I_{ON}/I_{OFF} by gate configuration and barrier modulation," in *IEDM Tech. Dig.*, Dec. 2011, pp. 16.2.1–16.2.4, doi: 10.1109/IEDM.2011.6131564.ISSN 2156-017X.

[15] S. Pregl, A. Heinzig, L. Baraban, G. Cuniberti, T. Mikolajick, and W. M. Weber, "Printable parallel arrays of Si nanowire Schottky-barrier-fets with tunable polarity for complementary logic," *IEEE Trans. Nanotechnol.*, vol. 15, no. 3, pp. 549–556, May 2016, doi: 10.1109/TNANO.2016.2542525.

[16] Y.-C. Wu and Y.-R. Jhan, "Introduction of synopsys sentaurus TCAD simulation," in *3D TCAD Simulation for CMOS Nanoeletronic Devices*. Singapore: Springer, 2018, ch. 1, pp. 1–17. [Online]. Available: https://www.springer.com/us/book/9789811030659

[17] S. A. Tawfik and V. Kursun, "Low-power and compact sequential circuits with independent-gate FinFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 60–70, Jan. 2008, doi: 10.1109/TED.2007.911039.

[18] Y. Liu *et al.*, "Cointegration of high-performance tied-gate three-terminal FinFETs and variable threshold-voltage independent-gate four-terminal FinFETs with asymmetric gate-oxide thicknesses," *IEEE Electron Device Lett.*, vol. 28, no. 6, pp. 517–519, Jun. 2007, doi: 10.1109/LED.2007.896898.

[19] M. H. Chiang, K. Kim, C. T. Chuang, and C. Tretz, "High-density reduced-stack logic circuit techniques using independent-gate controlled double-gate devices," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2370–2377, Sep. 2006, doi: 10.1109/TED.2006.881052.

[20] X. Zhang, J. Hu, and X. Luo, "Optimization of dual-threshold independent-gate FinFETs for compact low power logic circuits," in *Proc. IEEE 16th Int. Conf. Nanotechnol. (IEEE-NANO)*, Aug. 2016, pp. 529–532, doi: 10.1109/NANO.2016.7751552.
[21] M. S. Kim *et al.*, "Comparative area and parasitics analysis in FinFET and heterojunction vertical TFET standard cells," *J. Emerg. Technol. Comput. Syst.*, vol. 12, no. 4, Jul. 2016, Art. no. 38, doi: 10.1145/2914790.http://doi.acm.org/10.1145/2914790
[22] C. Auth *et al.*, "A 10 nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects," in *IEDM Tech. Dig.*, Dec. 2017, pp. 29.1.1–29.1.4, doi: 10.1109/IEDM.2017.8268472.ISSN 2156-017X.
[23] E. Sicard. (2017) *Introducing 7-nm Finfet Technology in Microwind*. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01558775/
[24] A. Guler and N. K. Jha, "Ultra-low-leakage, robust FinFET SRAM design using multiparameter asymmetric FinFETs," *J. Emerg. Technol. Comput. Syst.*, vol. 13, no. 2, Nov. 2016, Art. no. 26, doi: 10.1145/2988233.

Talha F. Canan (S'16) received the B.S. degree from the Department of Electrical and Electronics Engineering, Bilkent University, Ankara, Turkey, in 2015.

He joined Ohio University, Athens, OH, USA, in 2016 to commence his Ph.D. work on nanoscale CMOS integrated systems, logic devices, and interconnects for kilocore computing architectures. His current research interests include III–V and III–N semiconductor devices, avalanche photodiodes, thin-film transistors, and flexible electronic integration.

Savas Kaya (SM'07) received the M.Phil. degree from the University of Cambridge, Cambridge, U.K., in 1994, with a focus on polarization insensitive liquid crystal switches and the Ph.D. degree from the Imperial College of Science, Technology and Medicine, London, U.K., in 1998, with a focus on strained Si quantum wells on vicinal substrates.

He is currently a Professor with the Russ College of Engineering, Ohio University, Athens, OH, USA.

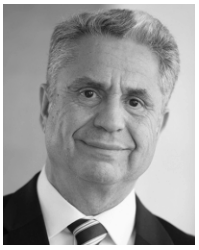
Avinash Karanth (SM'12) received the M.S. and Ph.D. degrees in electrical and computer engineering from The University of Arizona, Tucson, AZ, USA, in 2003 and 2006, respectively.

He is currently a Professor of electrical engineering and computer science with Ohio University, Athens, OH, USA. His current research interests include computer architecture, optical interconnects, chip multiprocessors, and network-on-chips.

Dr. Karanth is a member of the ACM.

Hao Xin (F'18) received the Ph.D. degree in physics from the Massachusetts Institute of Technology, Cambridge, U.K., in 2001.

From 2000 to 2003, he was a Research Scientist with Rockwell Scientific Company, Thousand Oaks, CA, USA. He is currently a Professor and the Director of the Cognitive Sensing Center, Electrical and Computer Engineering and Physics Departments, The University of Arizona, Tucson, AZ, USA.



Ahmed Louri (F'11) received the Ph.D. degree in computer engineering from the University of Southern California, Los Angeles, CA, USA, in 1988.

From 1988 to 2015, he was a Professor of electrical and computer engineering with The University of Arizona, Tucson, AZ, USA. He has been the David and Marilyn Karlgaard Professor with the Electrical and Computer Engineering Department, George Washington University, Washington, DC, USA, since 2015.