Evaluating the Scalability and Performance of 3D Stacked Reconfigurable Nanophotonic Interconnects

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***Abstract*—As we integrate hundreds of cores in the future, energy-efficiency and scalability of Network-on-Chips (NoCs) has become a critical challenge. In order to achieve higher performance-per-Watt than traditional metallic interconnects, researchers are exploring alternate energy-efficient emerging technology solutions. In this paper, we propose to combine two emerging technologies, namely 3D stacking and nanophotonics that can deliver high on-chip bandwidth and low energy/bit to achieve a high-throughput, reconfigurable and scalable NoC for many-core systems. Our simulation results indicate that the execution time can be reduced up to 25% and energy consumption reduced by 23% for Splash-2, PARSEC, SPEC CPU2006 and synthetic benchmarks for 64-core and 256-core versions.**

Keywords—Nanophotonics, NoCs, Reconfiguration.

I. INTRODUCTION

While Network-on-Chips (NoCs) design paradigm offers modular and scalable performance, increasing core counts leads to increase in serialization latency and power dissipation as packets are processed at many routers. Emerging technologies such as nanophotonic interconnects and 3D stacking are under serious consideration for meeting the communication challenges posed by the multicores. Nanophotonic interconnects provides several advantages such as: (1) bit rates independent of distance, (2) higher bandwidth due to multiplexing of wavelengths, (3) larger bandwidth density by multiplexing wavelengths on the same waveguide/fiber, (4) lower power by dissipating only at the endpoints of the communication channel and many more [1,2]. Similarly, 3D stacking of multiple layers have shown to be advantageous due to (1) shorter inter-layer channel, (2) reduced number of hops and (3) increased bandwidth density.

II. ARCHITECTURE & RESULTS

The proposed 3D-NOC architecture consists of 256 cores in 64 tile configuration on a 400 mm^2 3D IC. As shown in Figure 1, 256 cores are mapped on a 8 × 8 network with a concentration factor of four. From Figure 1(a), the bottom layer, called the *electrical* die, adjacent to the heat sink, contains the cores, caches and memory controllers. The upper die, called the optical die, consists of electro-optic transceivers which is driven by the cores via TSVs and four decomposed

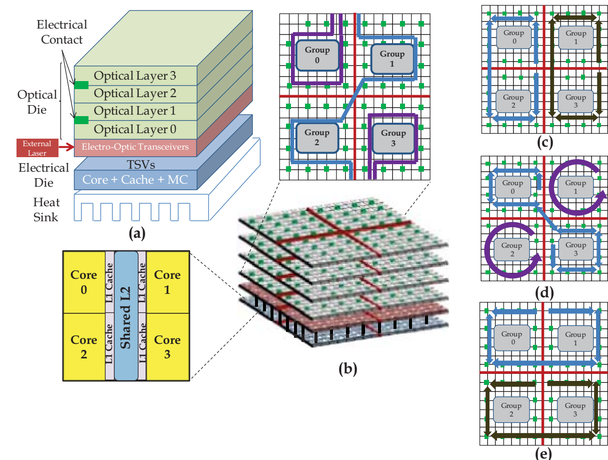

Fig. 1. Example of the proposed 3D stacked nanophotonic architecture.

nanophotonic crossbars. The top inset of Figure 1(b) shows the interconnect for layer 0 whereas Figures 1(c-e) show layers 1-3. We also provide electrical contact between layers 0/1 and 2/3 to tune ring resonators required for reconfiguration. The approach taken here is to couple between the optical layers through the use of vertically coupled ring resonators. In the proposed 3D layout, we divide tiles into four groups based on their physical location. Each nanophotonic crossbar is a 16 × 16 crossbar connecting all tiles from one group to another.

As future multicores will run diverse scientific and commercial applications, networks that can adapt to communication traffic at runtime will maximize the available resources while simultaneously improving the performance. To implement reconfiguration, we propose to include additional MRRs that can switch the wavelengths from different layers to create a reconfigurable network. Our simulation results indicate that the execution time can be reduced up to 25% and energy consumption reduced by 23% for Splash-2, PARSEC, SPEC CPU2006 and synthetic benchmarks for 64-core and 256-core versions.

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REFERENCES

[1] D. Vantrease and et.al, "Corona: System Implications of Emerging Nanophotonic Technology", ISCA-35, pp. 153-168, June 2008.

[2] Y.Pan and et. al., "Firefly: Illuminating Future Network-on-Chips with Nanophotonics," ISCA-36, June 2009.

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