Monopoles Loaded With 3-D-Printed Dielectrics for Future Wireless Intrachip Communications

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***Abstract*— We propose a novel antenna design enabled by 3-D printing technology for future wireless intrachip interconnects aiming at applications of multicore architectures and system-on-chips. In our proposed design we use vertical quarter-wavelength monopoles at 160 GHz on a ground plane to avoid low antenna radiation efficiency caused by the silicon substrate. The monopoles are surrounded by a specially designed dielectric property distribution. This additional degree of freedom in design enabled by 3-D printing technology is used to tailor the electromagnetic wave propagation. As a result, the desired wireless link gain is enhanced and the undesired spatial crosstalk is reduced. Simulation results show that the proposed dielectric loading approach improves the desired link gain by 8–15 dB and reduces the crosstalk by 9–23 dB from 155 to 165 GHz. As a proof-of-concept, a 60 GHz prototype is designed, fabricated, and characterized. Our measurement results match the simulation results and demonstrate 10–18 dB improvement of the desired link gain and 10–30 dB reduction in the crosstalk from 55 to 61 GHz. The demonstrated transmission loss of the desired link at a distance of 17 mm is only 15 dB, which is over 10 dB better than the previously reported work.**

***Index Terms*— 3-D printing, antennas, electromagnetic propagation, interconnect, intrachip communication, multiprocessor interconnection, network-on-chip (NoC).**

I. Introduction

THE continuing reduction in CMOS feature size has resulted in sub 10 nm (Intel just announced a 7 nm fab in Phoenix, Arizona [1]) which will allow integration of kilo-core (1000 cores) processors in the future multicore chips. However, as the width of traditional on-chip *RC* line interconnects also scales down, the extreme scaling poses a significant performance challenge for traditional on-chip interconnects: narrower metal interconnects are plagued with a larger intrinsic *R–C* time delay and energy losses due to higher resistive and capacitive parasitics [2]–[4]. Moreover, as the core counts keep increasing, traditional wired network-on-chip (NoC) solutions, which used to provide the required connectivity in multicore architectures, face increased latency, and power consumption [5]. Therefore, kilo-core on-chip interconnects are a very critical design challenge for scaling these architectures [2]–[4], [6], [7].

Wireless interconnects have been proposed as a promising complementary alternative to the traditional metallic-based *RC* line interconnects. Wireless links rely on electromagnetic waves propagating at the speed of light, which avoid the performance degradation, especially latency, caused by the traditional *RC* line interconnect scaling. Further, wireless links can provide cost-effective long-range and high-bandwidth direct links between distant cores, thus circumventing multihop latencies [5]. Consequently, Wireless NoCs (WiNoCs) are a promising alternative to cope with both the latency and power efficiency concerns of the future multicore architectures [8]–[10].

The design of on-chip antennas is one of the biggest challenges for wireless interconnects [11] due to the following two reasons. First, the CMOS substrate, i.e., the silicon substrate has a low resistivity (thus high loss) and a high dielectric constant [12]. When frequency reaches tens of gigahertz, silicon substrate attracts and confines most of the electromagnetic energy, making the antenna radiation efficiency thus gain very low [13], [14]. For example, in [15], 15 GHz on-chip transmitters, receivers, and zig-zag antennas have been demonstrated. The intrachip communication performance, however, is limited, mainly because of the inadequate gain of the antennas. At 15 GHz, the antenna pair suffer a high transmission loss of 45 dB for 3.2 mm separation [15]. Second, even without the impact from the silicon substrate, large path losses and undesired crosstalk between antennas may significantly limit the WiNoC performance.

To reduce the impact from the silicon substrate on on-chip antennas, a number of technologies have been proposed. In [16], a CMOS on-chip slot antenna at 140 GHz backed with an extremely thin cavity formed by two CMOS inner metal

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layers and vias in between is proposed. The cavity protects the electromagnetic energy from being absorbed by the substrate thus enhances the radiation efficiency of the slot antenna. However, the bandwidth of the antenna is only 5 GHz, which is mainly caused by the cavity's flatness. In [17], a high dielectric constant ($\varepsilon_r = 38$) rectangular dielectric resonator excited by an H-slot antenna is achieved based on the IBM SiGe5AM process. The gain of this antenna is 1 dBi at 35 GHz. However, the radiation is mainly toward the vertical direction, making it less attractive for intrachip communication that requires horizontal communication.

In this paper, we propose to use vertical quarter-wavelength monopoles on a ground plane at 160 GHz for wireless intrachip interconnects. The ground plane separates the silicon substrate from the antenna, eliminating the substrate effects and enhancing radiation efficiency. More importantly, well-designed artificial dielectrics surrounding the monopoles enabled by 3-D printing technology are employed to enhance the performance of desired wireless links and reduce the undesired crosstalk. The resulting antenna design leads to a more power-efficient and less interference-prone wireless interconnects. We conduct both a full-wave 3-D electromagnetic simulation and a proof-of-concept experimental design study to validate the proposed approach. To the best of our knowledge, this is the first work that proposes the use of the 3-D printing technology to design high-performance antennas for wireless interconnects aiming at multicore architectures applications.

This paper is organized as follows. Section II presents the NoC architecture, which utilizes wireless interconnect for long range intrachip interconnects. Section III explores the dielectric loading method for the vertical monopoles at 160 GHz as intrachip wireless interconnects; next, the design of a prototype at 60 GHz for the experimental validation is presented. Section IV presents the fabrication and measurement results, which demonstrate good agreement with the simulation results. Section V provides a detailed discussion centered on the latency comparison of the proposed wireless interconnects and traditional *RC* line interconnects. Finally, Section VI concludes the paper.

II. Network-on-Chip Architecture

The antenna structures proposed are for a novel optical-WiNoC (OWN) architecture for kilo-core computing that utilizes both optical and wireless interconnects [18]. Wireless interconnects reduce the hop count between the optically connected clusters, leading to improved performance and more efficient utilization of the finite wireless bandwidth. Our previous results indicate that OWN architecture consumes 30.36% less energy, and improves throughput by 8% over wireless-alone architectures and obtains 35.5% less area than optical-alone architectures [18].

The OWN architecture is a tile-based architecture with each tile consisting of four processing cores and their private L1 instruction and data caches, a shared L2 cache and a network interface or router. Each tile is located within a cluster, which consists of 16 such tiles (64 cores), as shown in Fig. 1. Four clusters form the 256-core OWN architecture,

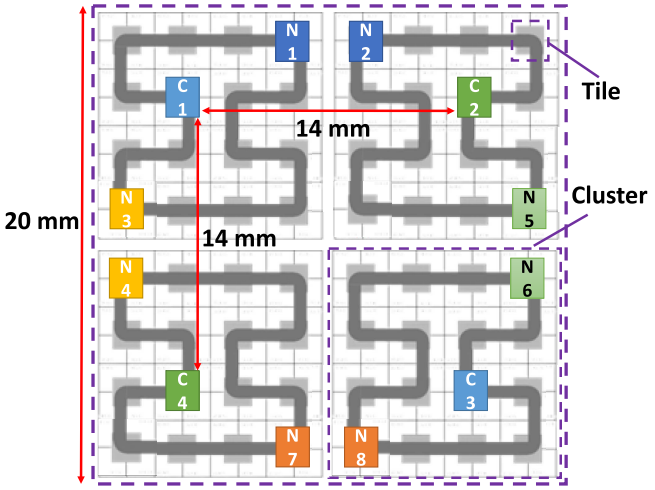

Fig. 1. 256-Core OWN architecture. Routers with the same color communicate with each other.

which has an area of about 20×20 mm^2 (note that the designs shown in this paper can be scaled to other chip sizes such as 50×50 mm^2). Intracluster communication is implemented using optical interconnects whereas intercluster communication is facilitated by 16 wireless links operating within 20 GHz bands, between 60 and 380 GHz.

To facilitate intercluster communication, we propose to use wireless routers N1–N8 and C1–C4 as illustrated in Fig. 1. Wireless router N1 (top-left cluster) communicates with N2 (top-right cluster); wireless router N3 (top-left cluster) communicates with wireless router N4 (bottom-left cluster) and so on. Therefore, wireless routers N1–N8 enable neighboring intercluster communication (same color). Wireless routers C1 (top-left cluster) communicates diagonally with C3 (bottom-right cluster) and C2 communicates with C4. That is to say, corner-to-corner (C2C) wireless links (i.e., C1-to-C3 and C2-to-C4) are desired, whereas edge-to-edge (E2E) wireless links (i.e., C1-to-C2, C2-to-C3, C3-to-C4, and C4-to-C1) are deemed undesired crosstalk/inference. This paper focuses on providing antenna solutions for wireless router C1–C4, which are at the vertices of a 14×14 mm^2 square. The antennas work at 160 GHz, which act as one frequency channel for the OWN architecture. Under the assumption of quadrature phase-shift keying modulation that allows up to 2 b/s/Hz spectral efficiency, 8 GHz frequency bandwidth is expected for the antennas so that 16 Gbps throughput is possible for the channel.

III. Design Methodology

A. 160 GHz Antenna Design for Intrachip Interconnect

In this section we preset the design of the vertical quarter-wavelength antennas operating at 160 GHz. In this case, the ground plane helps to eliminate the impact from the lossy silicon substrate. Such advantage is verified using an HFSS simulation with the model shown in Fig. 2(a). A monopole antenna (PEC) with a $\lambda_0/4$ length and a 0.1 mm diameter stands at the center of a 6×6 mm^2 ground plane (PEC). Beneath the ground plane is a 290 μm thick silicon substrate ($\varepsilon_r = 11.9$, $\mu_r = 1$, and $\rho = 10\ \Omega \cdot$ cm; standard

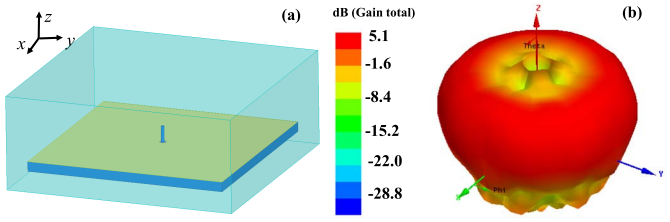

Fig. 2. (a) HFSS model of a quarter-wavelength monopole antenna on a finite ground (6×6 mm^2) in the air box (radiation boundaries). The blue part is the 290 μm thick silicon substrate. (b) Radiation pattern of the monopole antenna at 160 GHz.

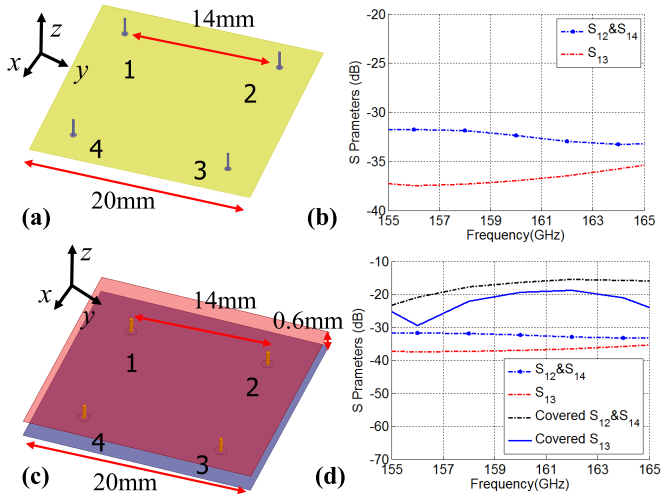

Fig. 3. (a) HFSS model of four quarter-wavelength monopole antennas on a finite ground. (b) S-parameters of the monopole antennas in (a). (c) HFSS model of four quarter-wavelength monopole antennas with a metallic cover 0.6 mm above the ground plane. The metallic cover could be included in the package of the silicon die. (d) S-parameters of monopole antennas with and without the metallic cover.

0.18 μm CMOS process substrate thickness). The simulation shows that the antenna has a gain of 5.1 dBi at 160 GHz, as illustrated in Fig. 2(b), which is close to the theoretical gain (5.19 dBi) of a quarter-wavelength monopole. The simulated radiation efficiency is 99.2%, showing very little loss caused by the silicon substrate. Compared with the previously reported on-chip zig-zag dipoles that have -8 to -10.5 dBi gain [13], the monopole antenna is free from the impact of the substrate effect and achieves much higher gain.

As illustrated in Fig. 1, the wireless routers are at the vertices of a 14×14 mm^2 square. An HFSS model corresponding to the WiNoC is setup, as illustrated in Fig. 2(a). The four monopoles are located at the vertices of a 14×14 mm^2 square. Each monopole is $\lambda_0/4$ (0.47 mm) long at 160 GHz with a diameter of 0.1 mm. The ground size is 20×20 mm^2. The silicon substrate has little impact on the antenna performance, as shown in the single monopole example in Fig. 3(a). Therefore, the substrate is not included in the model for the sake of computational efficiency. The simulation results are shown in Fig. 3(b). It is observed that S_{13} is smaller than S_{12}, which is due to the larger distance between Antenna 1 and Antenna 3. Next, a 20×20 mm^2 metallic cover is placed 0.6 mm above the ground plane to help confine radiation in the horizontal plane, as shown in Fig. 3(c). It can be observed in Fig. 3(d) that about 10 dB improvement is achieved for C2C and E2E wireless link gain.

To enhance the desired C2C link gain and suppress the undesired E2E crosstalk, dielectric loading technique based on 3-D printing technology can be utilized [19]. The space surrounding the monopoles (between the metallic cover and ground) is digitized into ideal dielectric blocks, i.e., unit cells with distinct dielectric constant ε_r as illustrated in Fig. 4(a). The inhomogeneity around the monopoles will be utilized to control the propagation of EM wave between the metallic cover and ground, which in turn enhance the desired links and suppresses the crosstalk.

For the 160 GHz antennas, each monopole is 0.36 mm long (slightly less than $\frac{1}{4}\lambda_0$) so that the resonance is in the 155–165 GHz range with the loaded dielectric. The dielectric loading space is discretized into 20×20 identical blocks, whose dimensions are $1 \times 1 \times 0.6$ mm^3. The ε_r of each block can be any value from 1.6 to 2.6 with a 0.25 increment. By optimizing the ε_r spatial distribution with genetic algorithm (GA), the goal of enhancing C2C antenna communication and reducing E2E antenna communication can be achieved in the targeting frequency range of 155–165 GHz. It should be noted that the relatively small ε_r range is chosen to restrict the optimization parameter space thus simplify the optimization problem.

The MATLAB-based GA code is utilized to control ANSYS HFSS for optimization of the ε_r distribution. To reduce the optimization parameters by a factor of eight, a symmetry of the ε_r distribution with respect to the x-axis, y-axis, and the diagonals as illustrated in Fig. 4(b) is applied. It should be noted that the E2E link gain is $S_{12} = S_{14} = S_{32} = S_{34}$ and the C2C link gain is $S_{13} = S_{24}$ under this symmetry. The GA optimization is defined as follows:

1) objective function: fitness value as large as possible (stop the optimization process when there is no significant improvement, e.g., Δ fitness < 0.3 after tens of generations);
2) fitness function: fitness $= [S_{13}(f) - S_{12}(f)]$, where $f \in [155, 165$ GHz$]$;
3) constraints: a ε_r range of 1.6–2.6 with a discretization of 0.1;
4) crossover probability and method: 100%; one-point crossover;
5) mutation probability: 0.1;
6) mutation type: generating a random ε_r.

A population size of 3 is used in the GA for efficient and parallel simulations. Although GA usually works well when the population size is large, we are able to achieve the desired results because the range of ε_r is not large. The optimized ε_r distribution is illustrated in Fig. 4(c). The optimization results of S-parameters are shown in Fig. 4(d)–(f). It is obvious that the optimized inhomogeneous dielectric distribution improves S_{13} (desired link) by 8–15 dB compared to the antennas with only metallic cover. Moreover, it suppresses S_{12} (undesired crosstalk) by 9–23 dB. Consequently, the loaded dielectrics help to boost the wireless link efficiency and reduce interference.

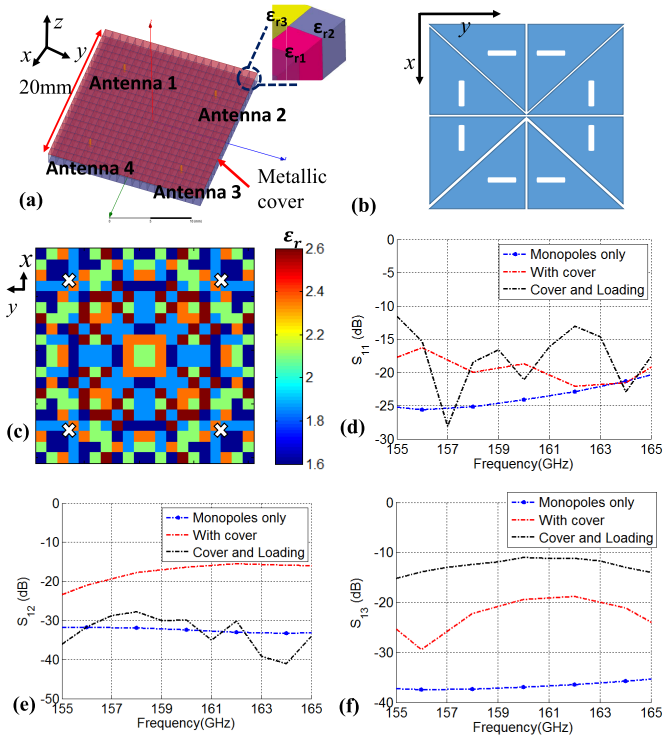

Fig. 4. (a) HFSS model of four quarter-wavelength monopoles on finite ground with both a metallic cover and unit cells (ideal dielectric blocks) with assigned distinct ε_r. (b) Symmetry used in the ε_r distribution to reduce optimization parameters by a factor of eight; the symmetry is with respect to the x-axis, y-axis, and the diagonals. (c) ε_r distribution surrounding the 160 GHz monopoles. The white crosses indicate the location of the monopoles. The S-parameters comparison of monopoles only, monopoles with metallic cover, and monopoles with both metallic cover and dielectric loading. (d) S_{11}. (e) S_{12}. (f) S_{13}.

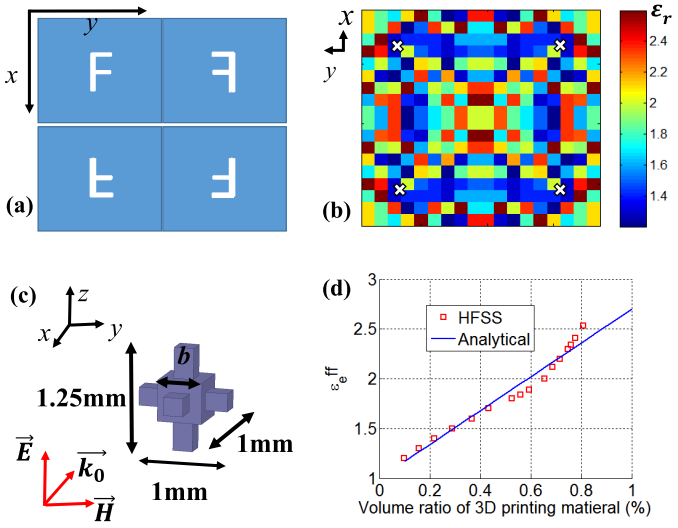

Fig. 5. (a) Symmetry used in the ε_r distribution to reduce optimization parameters by a factor of four. The symmetry is with respect to the x- and y-axes. (b) ε_r distribution surrounding the 60 GHz monopoles. The white crosses show the location of the monopoles. (c) Unit cell structure of the designed dielectric distribution. (d) Effective dielectric constant of unit cells with different polymer cube sizes based on the analytical calculation and HFSS simulation.

B. 60 GHz Antenna Prototype Design

As a proof-of-concept, an antenna prototype working at 60 GHz is designed and fabricated. The 20×20 mm^2 metallic cover is 1.25 mm above the ground. Four monopoles are located at the vertices of a 12×12 mm^2 square. The monopoles are 1 mm long, which is slightly less than $\lambda_0/4$ at 60 GHz. The diameter of the monopole is 0.23 mm. The monopoles are surrounded by 18×18 ideal dielectric blocks (i.e., unit cells) that have a size of $1 \times 1 \times 1.25$ mm^3, corresponding to $0.2\lambda_0$ at 15 GHz, which is a good compromise of effective medium approximation and printing accuracy. The ε_r of the unit cell range is 1.2–2.6 with a 0.1 discretization, which can be conveniently implemented using a 3-D printing technique that reported previously [20].

GA is used to optimize the dielectric constant distribution surrounding the monopoles. A symmetry of the ε_r distribution with respect to x- and y-axes as illustrated in Fig. 5(a) is used in the simulation such that $S_{13} = S_{24}$, $S_{12} = S_{34}$, and $S_{14} = S_{32}$, which reduces the optimization parameters by a factor of four. The GA optimization is defined similar to the 160 GHz optimization except for the following:

1) fitness function: fitness $= [S_{13}(f) - \max(S_{12}(f), S_{14}(f))]$, where $f \in [55, 61$ GHz$]$;
2) constraints: a ε_r range of 1.1–2.6 with a discretization of 0.1;

The optimized ε_r distribution is illustrated in Fig. 5(b).

Once the spatial ε_r distribution surrounding the monopoles is achieved, they are realized by 3-D-printed unit cell structures based on the effective medium approximation. The unit cell structure is shown in Fig. 5(c). It consists of the 3-D-printed polymer (dark blue part; $\varepsilon_r = 2.7$ and $\tan\delta = 0.02$ [20]) and air voids ($\varepsilon_r = 1$). The 3-D-printed polymer structure includes six pillars and a variable polymer cube with edge size b. The pillars in the x- and y-directions are to mechanically connect each neighboring unit cells. The z-direction pillar is to offer mechanical support for the top metallic cover. The cross section of the pillars is 0.22×0.22 mm^2 so that they are small enough to avoid impacting much the effective dielectric property control while providing adequate mechanical strength for the structure. By changing b, or the filling ratio of the polymer material in the unit cell (i.e., mixing polymer and air at different ratios), effective ε_r from 1 to 2.7 can be obtained. The approximated permittivity of a unit cell is calculated by the analytical effective medium approximation based on the polymer filling ratio f using $\varepsilon_r = \varepsilon_p \cdot f + 1 \cdot (1 - f)$, where ε_r is the effective relative permittivity of the unit cell and ε_p is the relative permittivity of the polymer material [20]. Next, based on the Nicholson–Ross–Weir method [21], [22], the calculated effective permittivity is verified by finite-element simulations using HFSS software. Fig. 5(d) plots the effective relative permittivity extracted from the simulated S-parameters and that calculated from the filling ratio equation, with respect to the filling ratio f. It should be noted that the unit cell simulation assumes an incident plane wave with the E field in the z-direction propagating in the $-x$-direction, as illustrated in Fig. 5(c). Due to the symmetry of the unit cell structure in the x- and y-directions, the unit cell's effective dielectric constant (ε_{eff}) should be isotropic. Once the unit cell designs

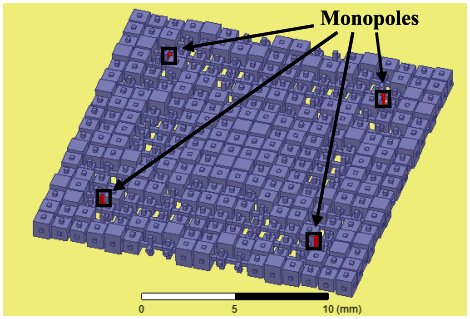

Fig. 6. HFSS model of the 60 GHz antenna prototype showing the monopoles and 3-D-printed polymer structure.

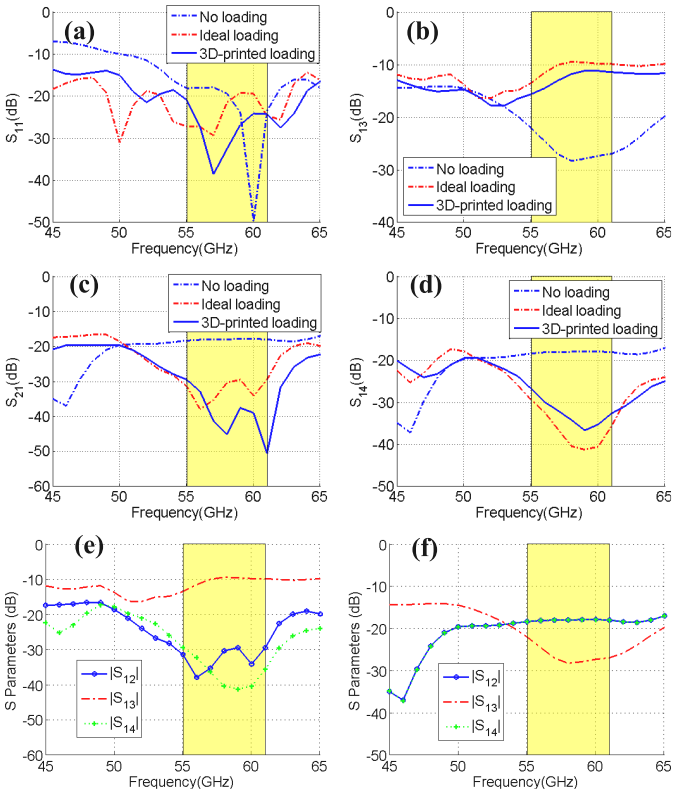

Fig. 7. S-parameters comparison of the no loading, the ideal dielectric blocks loading, and the 3-D-printed polymer loading cases. (a) S_{11}. (b) S_{13}. (c) S_{21}. (d) S_{14}. (e) S-parameters of the monopoles loaded with ideal dielectric blocks. (f) S-parameters of the no loading case.

are completed, the entire 3-D-printable antenna system is modeled in HFSS as illustrated in Fig. 6.

The optimized results are shown in Fig. 7(a)–(f), in which three cases are compared: the no loading case where there is no dielectric loading around antennas, e.g., Fig. 3(c); the ideal dielectric blocks loading case where the antennas are surrounded by the unit cells assigned by the desired dielectric constant, i.e., Fig. 4(a); the 3-D-printed polymer loading case where the antennas are surrounded by the entire printed dielectric structure including dielectric polymer and pillars, i.e., Fig. 6. Fig. 7(a) shows that the reflection coefficients are below −10 dB from 55 to 61 GHz for all three cases. The antenna's −10 dB impedance bandwidth becomes slightly larger after dielectric loading from 45 to 65 GHz. It is observed

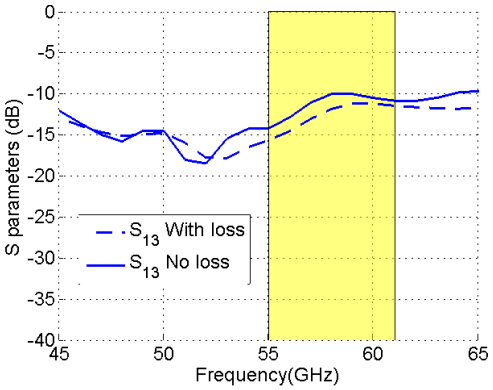

Fig. 8. S_{13} comparison of the dielectric loading with and without dielectric loss in the model ($\tan\delta = 0.02$ versus $\tan\delta = 0$).

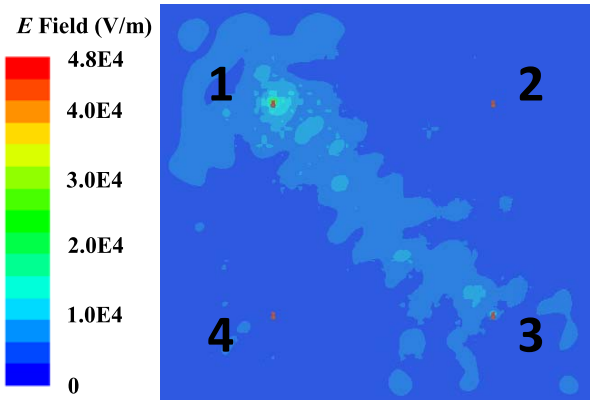

Fig. 9. Simulated E field (complex magnitude) distribution 0.5 mm above the ground plane when antenna 1 is excited at 60 GHz. The red dots are the locations of antennas. This figure shows that directional propagation is achieved between antenna 1 and antenna 3.

in Fig. 7(b) that the loaded dielectric boosts S_{13} by 10–18 dB from 55 to 61 GHz. The undesired crosstalk S_{21} and S_{14} are attenuated by 10–30 dB, as shown in Fig. 7(c) and (d). Fig. 7(e) shows that the figure of merit $= (S_{13} - S_{12})$ is 10–20 dB from 55 to 61 GHz, in comparison with −10 to −3 dB of the no loading case, as shown in Fig. 7(f). Good agreement between the ideal dielectric blocks model and the 3-D-printed polymer model can also be observed. Moreover, the dielectric loss caused by the loaded dielectrics is also investigated in the simulation. As shown in Fig. 8, the dielectric loss leads to about 1 dB degradation of the C2C link gain S_{13}, which is acceptable.

The simulated E field distribution (complex magnitude) in the xy plane 0.5 mm above the ground plane at 60 GHz is shown in Fig. 9. When antenna 1 is excited, electromagnetic power travels toward antenna 3 thus the C2C link gain is improved and E2E link gain is reduced. Fig. 10 shows the surface current distribution (complex magnitude) on the ground plane at 60 GHz. It can be observed that the current also concentrates on the diagonal path. If we consider the structure as a parallel plate waveguide, the lowest cutoff frequency for TM or TE modes is 120 GHz and thereby only TEM wave can propagate at 60 GHz. To verify this, the vector E field

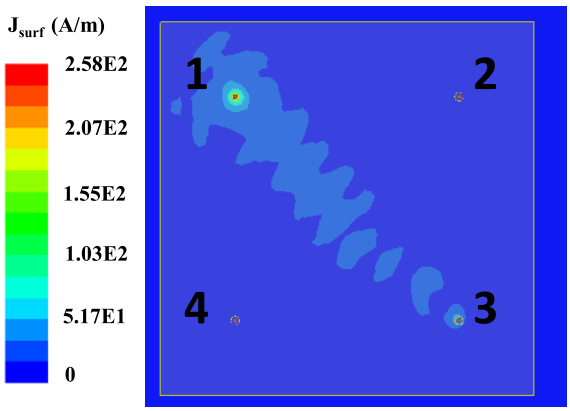

Fig. 10. Simulated surface current distribution (complex magnitude) on the ground plane. The yellow, half-transparent square shows the location of the metallic cover. The red dots are the locations of antennas. This figure shows that directional propagation is achieved between antenna 1 and antenna 3.

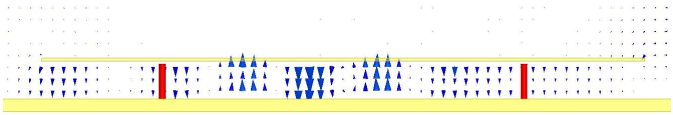

Fig. 11. Simulated vector E field between the metallic cover and ground on the xoz plane at 60 GHz. (The dielectric structure is hidden to better illustrate the field distribution.)

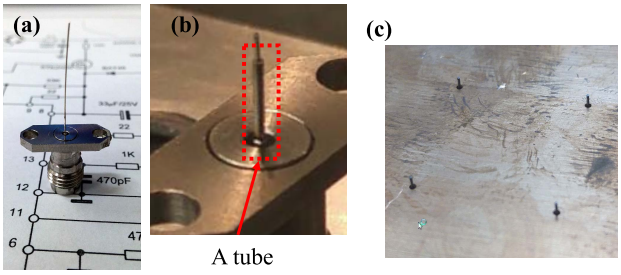

Fig. 12. (a) V-connector with the pin soldered. (b) Pin is inserted into the tube, which acts as a positioner during connectors' attachment to the ground to make sure that the pins are at the center of the holes. (c) Fabricated four monopoles on the ground plane.

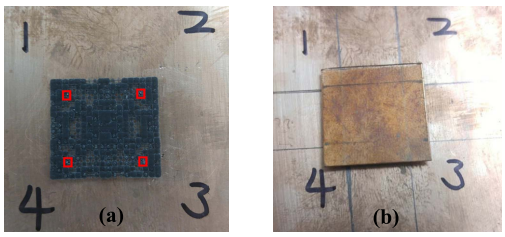

Fig. 13. (a) Four monopoles (indicated by the red squares) with the 3-D-printed polymer surrounding. (b) Final antenna structure with the metallic cover. The ground is 152.4 × 152.4 mm^2 and 0.4 mm thick. The dielectric is 18 × 18 × 1.25 mm^3. The four monopoles are at vertices of a 12 × 12 mm^2 square. The top metallic cover has a dimension of 20 × 20 × 0.4 mm^3.

in the xoz plane at 60 GHz is plotted in Fig. 11. It can be observed that the electric field is mostly in the z-direction.

IV. Fabrication and Measurement

A. Fabrication

The conductor part of the antenna prototype (monopoles) is fabricated by precision machining. The monopoles are coaxially fed by 1.85 mm (V) connectors through holes in the ground plane. Four holes ($\Phi = 0.51$ mm) are drilled at the center zone of a piece of copper sheet (152.4 × 152.4 mm^2; 0.4 mm thick). Four V-connectors accepting 0.23 mm diameter pins are utilized for antenna feeding. Pins with a diameter $\Phi = 0.23$ mm are inserted into the connectors' sockets and carefully soldered to fixate the pins into the sockets, as shown in Fig. 12(a). Next, the V-connectors are attached to the ground via silver epoxy and nonconductive adhesive for electrical and mechanical connection, during which metallic tubes ($\Phi_{in} = 0.254$ mm and $\Phi_{out} = 0.45$ mm) are set in between the pins and holes to help put the pins at the centers of the holes, as illustrated in Fig. 12(b). Afterward, the tubes are removed and pin trimming is performed to obtain 1 mm long monopoles. The finally fabricated monopoles are illustrated in Fig. 12(c).

Additive manufacturing (AM), or 3-D printing technique, is utilized to fabricate the dielectric blocks surrounding the monopoles. AM enables low cost and rapid prototyping of arbitrary 3-D structures. Multiple applications in electromagnetics have been reported involving different types of AM methods [23]. In this paper, the 3-D polymer jetting technique is employed to implement the proposed design. Previously demonstrated electromagnetic components include electromagnetic bandgap structures [24], terahertz (THz) electromagnetic crystal horn antennas [25], THz waveguides [26], holograms [27], Luneburg lens antennas [20], and dielectric reflectarray antennas [28].

A commercial polymer jetting 3-D printer, Objet Eden 350, is utilized to fabricate the dielectric part. The resolution is as fine as 84 μm × 42 μm × 16 μm. The printing process is as follows. First, the structure information is sent to the printer controller in a CAD file. Next, the controller converts the structure information into a series of 16 μm thick layered slices. The layer information is then sent to the printer. According to the received data, printer heads print a layered polymer structure. The jetted polymer is cured immediately by the ultraviolet lamps on the print heads. In a layer-by-layer fashion from bottom to top, a 3-D structure is finally produced. Eden 350 allows simultaneous printing of two types of materials conveniently, in this paper, specifically, the 3-D-printed polymer material (VeroBlackPlus RGD875) and the support material (FullCure 705). The support material fills in any gap and prevents the polymer from drooping during printing. Once the entire structure is printed, the support material can be removed easily by high-pressure water spray. Fig. 13(a) shows the 3-D-printed polymer structure. The complete antenna prototype with the metallic cover is shown in Fig. 13(b).

B. Measurement Results

The measured S_{11} of the monopoles only case is illustrated in Fig. 14. It is observed that the measured resonance frequencies are lower than those of simulation. This is due to the extra length of the monopoles as a result of fabrication inaccuracies. It is discovered that the measurement results are

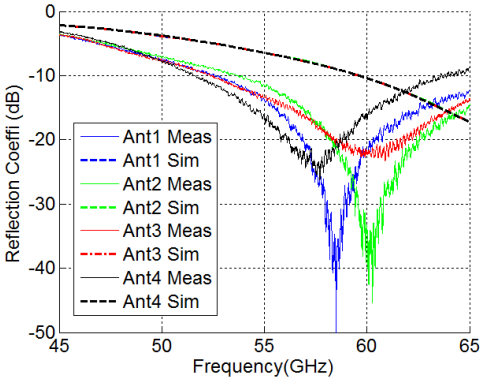

Fig. 14. Measured reflection coefficients of the monopoles only case in comparison with simulation results.

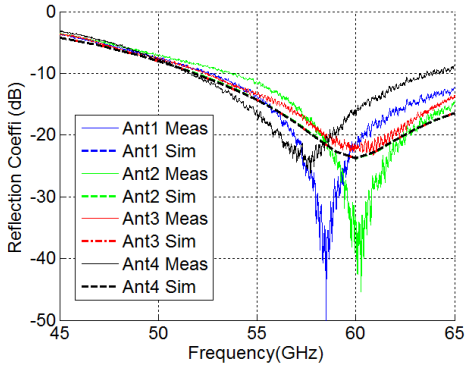

Fig. 15. Measured reflection coefficient of the monopoles only case in comparison with the simulation results of 1.16 mm long monopoles.

closest to the simulation results of 1.16 mm long monopoles, as shown in Fig. 15. S_{12}, S_{34}, S_{14}, S_{32}, S_{31}, and S_{24} are then measured and compared with the 1.16 mm long monopole simulation results, both with and without the dielectric loading and the metallic cover, as depicted in Fig. 16. In general, good agreement between the measurement and simulation results is observed. The discrepancies, especially the resonant frequency shift of S_{14} and S_{32} in Fig. 16(c) and (d), are likely due to the position inaccuracies of the loaded dielectric and top metallic cover with respect to the antennas. In the experiment, it is quite hard to control the relative position accurately. To understand this better, simulation results for the case that the loaded dielectric is offset by (-0.3, 0.3, and 0 mm) and the metallic cover is offset by (0.5, 0.5, and 0 mm) are shown in Fig. 17. It can be observed that S_{14} and S_{32} agree better with the measurement results.

Moreover, Fig. 16(e) and (f) shows that transmission loss as small as 15 dB is achieved at 60 GHz at a distance of 17 mm in the experiment, in comparison with 22.2 dB calculated by the Friis transmission equation for 60 GHz monopoles and the reported 25 dB at 60 GHz at a distance of 15 mm in [29] using zig-zag antennas. The experimental results have substantiated previous analysis and demonstrated the improvement in the desired links and suppression in crosstalk from 55 to 61 GHz.

V. Analysis and Discussion

Electromagnetic wave has slower propagating velocity in dielectrics than in air. Therefore, more time delay is expected

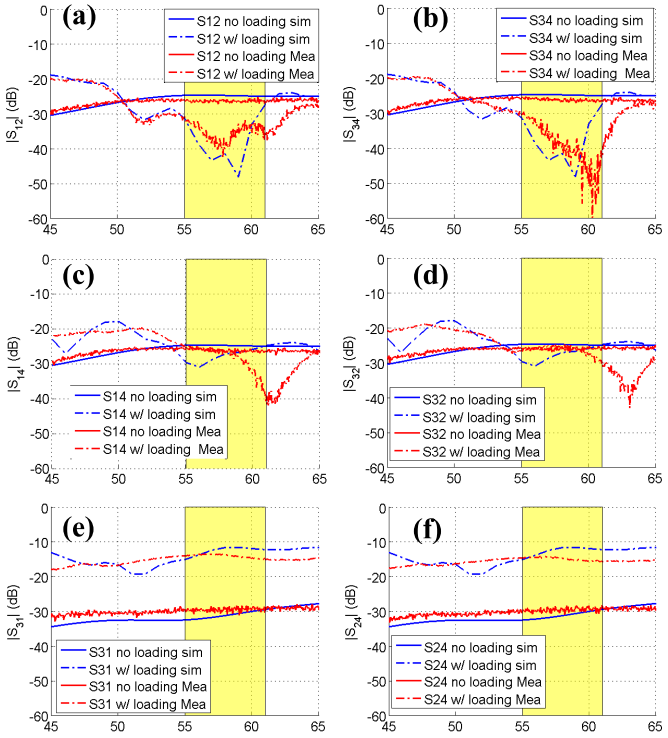

Fig. 16. Measured S-parameters of the fabricated monopoles in comparison with the simulation, with and without dielectric loading or metallic cover. (a) S_{12}, (b) S_{34}, (c) S_{14}, (d) S_{32}, (e) S_{31}, and (f) S_{24}.

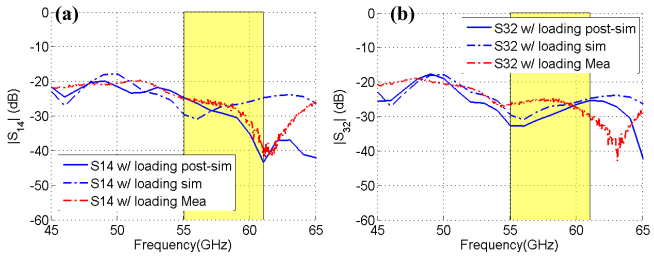

Fig. 17. Simulated S-parameters when the loaded dielectric is offset by (-0.3, 0.3, and 0 mm) and the metallic cover is offset by (0.5, 0.5, and 0 mm). (a) S_{14} and (b) S_{32}.

for antennas surrounded by dielectrics compared with those in air. In this section, a quantitative comparison of the delay between the traditional *RC* line interconnects and the dielectric loaded antennas is performed.

The larger time delay in traditional IC interconnect is due to the increased resistance as a result of interconnect scaling. A study of the interconnect delay has been reported in [3]. Taking 1 mm path as an example, the *RC* delay is ~80 ps for the 500 nm process (heavily doped silicon); for the 35 nm process (Cu, low k), about 250 ps delay is experienced. In comparison, the maximum delay for the wireless interconnect based on the proposed method is only $\tau = (l\sqrt{\varepsilon_r}/c) = 5.5$ ps where $l = 1$ mm is the distance between antennas, c is the speed of light, and $\varepsilon_r = 2.7$ is the maximal possible dielectric constant of the dielectric loading. That is to say, for 1 mm distance, the wireless interconnect will be 50 times faster than the *RC* line interconnect for

the 35 nm process. Moreover, the *RC* delay is proportional to the square of the distance [3]. In comparison, the wireless interconnect experiences delay proportional to the distance. Therefore, for larger distance, e.g., 17 mm communications, the wireless interconnect with loaded dielectric features about 850 times less delay compared to the *RC* line interconnect. In conclusion, the wireless interconnect with loaded dielectric is advantageous with significantly reduced time delay.

Some interesting aspects of this paper are worth further investigations. First, the experimental validation of monopole antennas on chip is desired. One possible method is the direct ink writing of 3-D metal structure [30]. Second, this paper may lend itself to reconfigurable wireless interconnect if a tunable dielectric material is available for loading and dynamic control.

VI. Conclusion

Vertical quarter-wavelength monopoles surrounded by optimized dielectric distribution are proposed for future intrachip wireless interconnects. As an example, the dielectric constant distribution surrounding four 160 GHz monopoles is optimized by GAs to improve the desired wireless link and suppress crosstalk. The simulation shows that the desired link is improved by 8–15 dB and the crosstalk is reduced by 9–23 dB from 155 to 165 GHz with our design. As an experimental proof-of-concept, a 60 GHz prototype is designed, fabricated, and measured. The 3-D printing technology is utilized to realize the designed ε_r distribution based on effective medium approximation, which features fast and convenient prototyping. The measurement results agree well with the simulation results, which demonstrate 10–18 dB improvement in the desired links and 10–30 dB reduction in crosstalk from 55 to 61 GHz. The transmission loss as small as 15 dB is achieved at 60 GHz at a distance of 15 mm in the experiment, in comparison with 22.6 dB calculated by the Friis transmission equation for 60 GHz monopoles and the reported 25 dB at 60 GHz at a distance of 15 mm in [29] using zig-zag antennas. This paper demonstrates that future wireless intrachip communication could benefit from 3-D-engineered dielectric loading as part of the antenna design methodology. It also unveils the promising potential of the additive 3-D printing technology in wireless communication.

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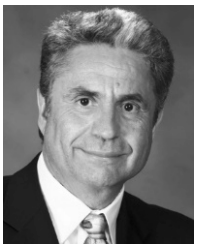

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