On-Chip Photonic Interconnects for Scalable Multi-core Architectures

Avinash Karanth Kodi[1], Randy Morris[1], Ahmed Louri[2] and Xiang Zhang[2]
[1]*School of Electrical Engineering and Computer Science, Ohio University, Athens, OH 45701*
[2]*Electrical and Computer Engineering, University of Arizona, Tucson, AZ 85721.*
E-mail: {kodi,rm700603}@ohio.edu, louri@ece.arizona.edu, zxkidd@gmail.com

Abstract

In this paper, we propose PROPEL, a photonic network-on-chip (NoC) that improves performance and power with energy-efficient opto-electronic components for future chip multiprocessors (CMPs). Our analytical and simulation results indicate that PROPEL improves throughput and reduces power over optical and electrical networks for various traffic traces while requiring fewer photonic components and devices.

1. Introduction

In this paper, we propose PROPEL - a power and area-efficient, high-performance NoC architecture targeting future 22nm technology node with 64 cores. The proposed architecture uses optical interconnects for long distance inter-router communication and electrical switching at the routers. This reduces the power dissipation on long inter-router links while electrical switching provides flow control to prevent buffer overflow. PROPEL uses dimension order routing (DOR) by traversing in both X and Y directions with an intermediate electrical conversion.

2. Architecture and Results

Figure 1 shows the proposed architecture. The proposed off-chip broadband light source will generate few wavelengths. By transmitting a continuous optical signal in the x- and y- direction simultaneously, the optical signal can be modulated at the optical transmitters. The figure shows 4 tiles combined together to form a super-tile. A tile is comprised of a processing core and its L2 cache. This grouping reduces the cost of the interconnect as every core does not require lasers attached and facilitates local communication through cheaper electronic switching. The number of wavelengths required is equal to the maximum number of super tiles in the x- or y-direction. Each super-tile consists of dual-set (x and y) photonic transceivers and an electronic switch. It takes a maximum of 2 hops to traverse any-to-any super tile, one hop in the x-dimension and one hop in the y-dimension. For inter super-tile communication, the static routing and wavelength allocation (RWA) involves selective merging of different wavelengths from various super-tiles into separate channels thereby maximizing the bandwidth (wavelength division multiplexing) and re-using the same wavelengths on different waveguides (space division multiplexing).

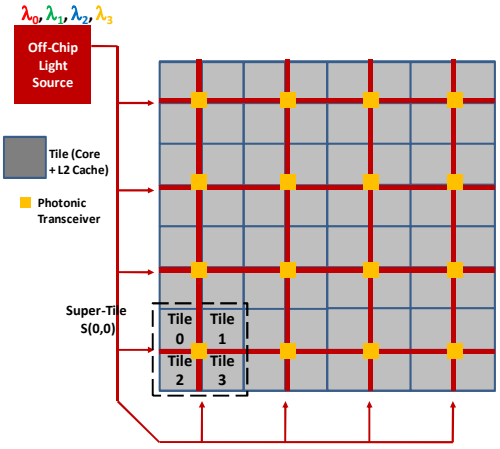

Figure 1: Proposed PROPEL architecture.

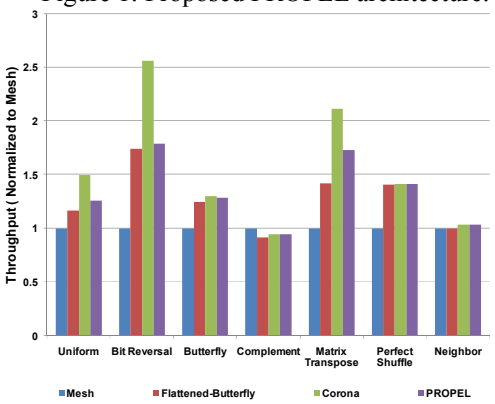

Figure 2: Throughput comparison.

Figure 2 shows the performance of PROPEL when compared to other competing electrical and optical NoC topologies including Mesh, Flattened Butterfly, CORONA and PROPEL. Although PROPEL significantly reduces the optical hardware complexity (components), its performance is comparable and even better than other competing technologies. For a more detailed report on PROPEL and its performance please see [2].

3. References

[1] J.D. Owens, et.al. "Research Challenges for On-Chip Interconnection Networks,"IEEE Micro, pp. 96-108, 2007.
[2] http://ouace.cs.ohiou.edu/~avinashk/propel.pdf

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