Sub-THz Tunable Push-Push Oscillators with FinFETs for Wireless NoCs

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***Abstract*—This paper investigates the properties of sub-THz compact tunable push-push oscillator in 45 nm FinFET technology. The push-push oscillator is designed to operate at 250 GHz in a modified cross-coupled LC topology. Commanding the FinFET gates separately in independent-mode bestows the push-push oscillator with a simple and efficient means for ∼5 GHz tunable performance without external varactors. Moreover, due to the increased transconductance, the stability criteria of oscillation is much relaxed in FinFET based design compared to that of an identical design in single gate MOSFET. No external capacitors are used to realize the LC tank unlike in conventional LC oscillator design. The higher gate-source capacitance of the FinFET is conveniently utilized to substitute for the external capacitor thus reducing parasitics and raising the resonant frequency. The phase noise of the oscillator varies from -82 to -76 dBc/Hz at 1 MHz offset between 0 V and 1 V back gate bias. The compact and tunable characteristics of the proposed sub-THz oscillator, make it ideally suitable for applications such as on-chip wireless interconnects required for kilo-core computing that have hard limits on area and power but requires precision tuning and high bandwidth for extremely fast data rates.**

I. Introduction

Novel circuit architectures with reduced complexity and higher efficiency in sub-THz frequency range are feasible as we progress with semiconductor technologies beyond CMOS devices. In the deca-nano regime, the 'traditional' single-gate MOSFETs have been replaced by a vareity of 3-D multi-gate devices [1]- [3]. These multi-gate nano-scale transistors can effectively control the channel from multiple sides instead of the top gate as in the case of conventional MOSFET architecture. The ability to alter channel potential by multiple gates (i.e double, triple, surround) provides a relatively easier and robust way to control the channel electrostatics, reducing the short channel effects and leakage concerns considerably. With the multiple gate boundary conditions, efficient tunable analog performance is possible by independently driving FinFET dual gates developed originally for enhancing digital performance via symmetrically-biased (common-mode) operation. Moreover, exploration of such analog circuits have become even easier and more practical, with the recent introduction of BSIM-IMG model that has been developed specifically for independent gate (IG) operation. Using the novel BSIM-IMG model, in the present paper we explore one such compact and efficient tunable analog circuit: A push-push oscillator.

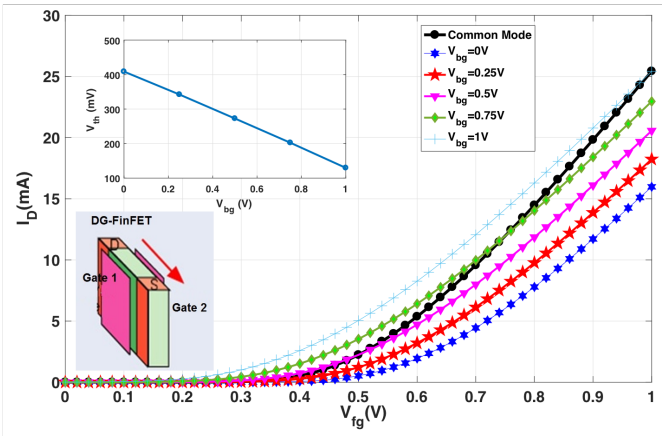

Fig. 1. I_D-V_{fg} characteristics of an n-type Independent ($V_{bg} \neq V_{fg}$) and Common ($V_{bg} = V_{fg}$) Mode DG transistors with BSIM-IMG FinFET. The top left inset shows the resulting shift in the front gate threshold while the bottom left shows tye structure of an independent mode DG-FinFET.

BSIM-IMG model is developed using surface-potential approach for the conduction channel, which is ideally suited for an accurate and systematical study of the FinFET based push-push oscillator circuit. The latest version (102.8.0) of the BSIM-IMG models the IG-FinFET structure as a four terminal device with source, drain, front and back gate contacts [4]. The transfer characteristics (I_D-V_{fg}) of an IG-FinFET are shown in Fig. 1, which relates the change in drain current with the front gate voltage for different back gate biases. The common mode characteristic (when the two gates are tied together) has also been plotted for comparison. Although common-mode has a higher g_m, it can not be tuned. The tunable threshold of the DG-FinFET can be observed from the upper inset of Fig. 1.

The proposed tunable push-push oscillator is designed especially for sub-THz, ultra-compact and low-power applications such as found in sensor networks and on- or off-chip wireless communications, where area and power are severely limited and accurate channel tuning and reconfiguration may be necessary. The requirement of ultra-high bandwidth and efficient wireless data transfer within the multi-core chip networks place particularly stringent demands in the design of sub-THz oscillator such as the topology proposed here.

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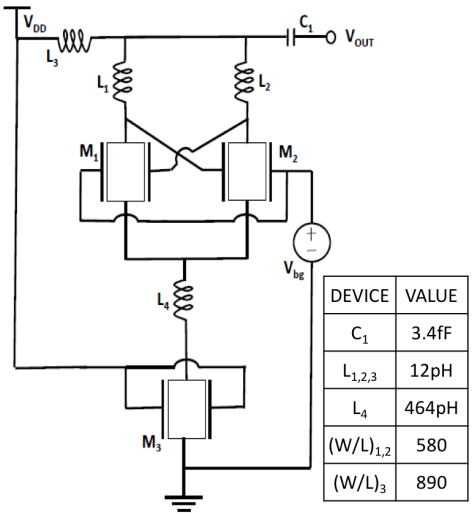

DEVICE	VALUE
C_1	3.4fF
$L_{1,2,3}$	12pH
L_4	464pH
$(W/L)_{1,2}$	580
$(W/L)_3$	890

Fig. 2. The modified push-push oscillator designed with 45-nm FinFETs.

Earlier works involving a series of radio frequency transceiver components have been studied in the FinFET technology, and their behavior have been reported in [5]. This list includes various lower frequency relaxation oscillators for baseband circuitry, 60GHz capable cross-coupled LC and quadrature oscillators as well as a recent mm-wave *Colpitts* oscillator topology [6]. The study of the characteristics of the push-push oscillator in this paper pushes the oscillator design with FinFETs to the sub-THz realm, which has not been explored before. Finally, the use of newly available BSIM-IMG model for oscillator design is another novel aspect of this work, indicating the potential of BSIM-IMG for FinFET-based analog circuit design.

II. Push-Push Oscillator Design

Push-push oscillators are mostly implemented by combining anti-phase balanced structures and extracting the second or higher harmonic signals from the virtual ground where the anti-phase fundamental signals cancel out. An impedance matching filter network designed at the second or higher harmonic frequencies is used to extract these harmonics. In this paper, a similar push-push oscillator with cross-coupled differential negative resistance element is implemented at 45 nm FinFET technology. The oscillator is a modified version of the oscillators reported in [7], [8].

To achieve higher operating frequency, one must minimise L_1, L_2 and the external capacitors used for resonance in any conventional LC cross-coupled oscillator. However, as this is attempted, the effective impedance due to the inductor increases while the parasitic capacitance associated with L_x grows. Hence, the inductor's parasitics establishes an upper limit: Its capacitive effect counteracts the minimization of external capacitances and ultimately affects the oscillation frequency in a way such that there is no significant increase in the oscillating frequency even with decreasing capacitances. Along with the impact on the oscillation frequency, it also affects the symmetry of the voltage swing. The inductor L_3 resonate with the device parasitics at the second harmonic frequency to get the desired oscillation at the output. The inductor L_4 filters out any RF signal from passing it to the transistor M_3 which acts a current source and in saturation. The values of the components used in the design of the circuit is given in Fig.2.

To reduce any non-linear effects and increase the frequency of operation, all external capacitors excepting the DC blocking capacitor C_1, have been removed from the design. The gate-source and/or gate-drain capacitance of the FinFETs, which is inherent to the device and typically much larger than the single-gate conventional MOSFETs, can be substituted for any external capacitors at the drain contacts.

The use of IG-FinFET is particularly beneficial in establishing a more relaxed frequency criterion for the oscillator, as compared to the conventional single gate, because of relatively higher $g_m = g_{m1} = g_{m2}$. In fact, when the two gates are joined the transconductance is at least doubled, and the oscillation criterion of the common-mode device reduces to

$$g_m R_S \geq \frac{1}{2} \tag{1}$$

where, R_S is the resistive loss of the inductors L_1 and L_2 [9]. Alternatively, a higher g_m can be also used to reduce the dimensions of the L_1 and L_2 or reduce R_S further. Another advantage in using FinFETs in the push-push design is related to the dimensions of M_3 that must be optimized to sink the current from M_1 and should remain in saturation. The higher g_m of M_3 can be used to reduce the area of this transistor, which also reduces parasitics. Finally, a 45nm FinFET is preferred over smaller L_{gate}=32nm and L_{gate}=22 nm counterparts in the present design. It is found that lower body thickness (larger parasitic capacitors) and higher thresholds of smaller transistors offer little returns in oscillation frequency, while reducing the tunable range considerably.

III. Simulation Results

Prior to circuit simulation, electromagnetic simulation of the inductor with ADS Momentum (from Keysight) was performed to study its behaviour at sub-THz frequency for reliability. The reflection loss of the inductor in the frequency range of interest is much less than 10% as can be observed from Fig. 3. The quality factor, Q, which determines the loss of the inductor and the variation of inductance with the frequency is also available in the figure. The S-parameters obtained from the electromagnetic simulation of the inductor is imported to Cadence Spectre RF to perform the circuit simulation of the complete oscillator, improving accuracy and realism of the proposed circuit.

The oscillation frequency has been studied for different back gate bias (V_{bg}) conditions which range from 0 to -1 V. The oscillation frequency at the -1 V bias condition can be observed from Fig. 4, which shows the power spectral density (PSD), to be 250 GHz. The variation in frequency with the different back gate bias conditions is provided in Fig. 5 along with total DC power dissipation, RF output power and the drain efficiency. Hence, the unique tunability achieved with

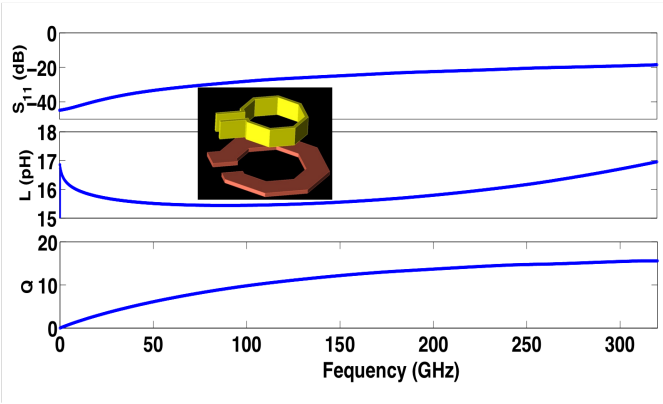

Fig. 3. The electromagnetic simulation of the inductor depicting the reflection loss, inductance and the quality factor (Q) over the frequency upto 320 GHz. The inductor 3D image in ADS momentum is shown in the inset. The metal 1 (in yellow) is the inductor and metal 8 (in orange) is the ground plane

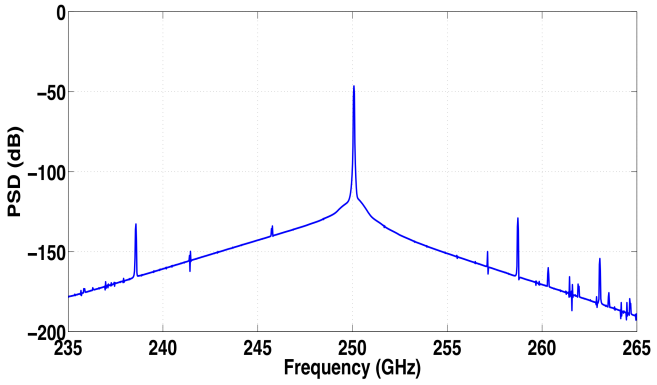

Fig. 4. The PSD of the DG-FinFET push-push oscillator after importing antenna S-Parameters from electromagnetic simulation.

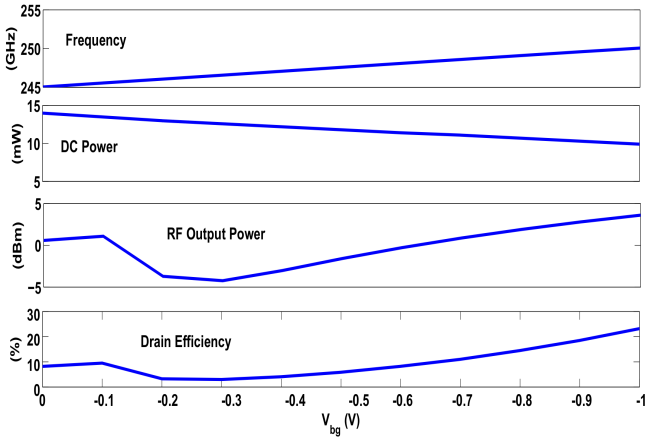

Fig. 5. Variation of oscillation frequency, DC and output power dissipation and drain efficiency for different back gate bias.

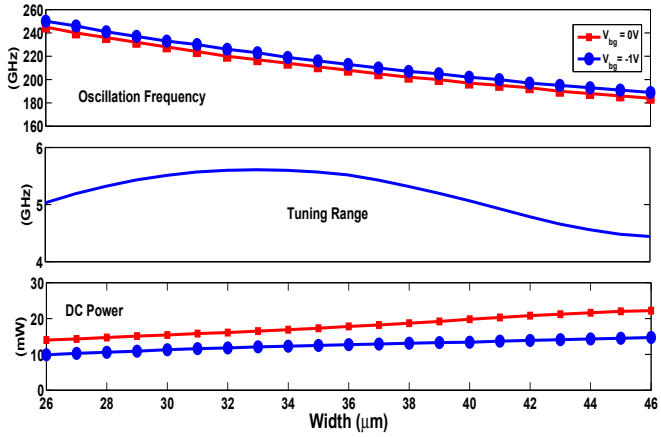

Fig. 6. Variation of oscillation frequency, tuning range and DC power dissipation with different transistor widths for the two extreme back gate bias conditions. The tuning range is the difference in oscillation frequency at these extremes.

these novel transistors are not only limited to frequency but extended to power consumption as well. As can be observed from Fig. 5, both the DC power dissipation and the output power increase linearly after reaching the back gate threshold of 0.3 V. The drain efficiency of the oscillator also depicted in Fig. 5 varies between 10% & 20%. The DC supply is kept at 1 V. The width of the transistors, M_1 & M_2 is optimized for least power dissipation and highest tuning range. As can be observed from Fig. 6 the DC power dissipation increases when the width of the transistor increases beyond 26 μm. Although the tuning range achieves a maximum value at a width of 33 μm the oscillation frequency is not at its peak at this device width. The frequency of oscillation is nearly 250 GHz when the device width is kept at 26 μm although the tuning range (Fig. 6) is not at its peak. The phase noise is achieved at 250 GHz frequency at the width of 26 μm. Hence, for all the analyses, the width of these transistors are kept at 26 μm for optimal performance. It can be noted the oscillation severely distorts when the width is kept below 18 μm.

At the device width of 26 μm, the oscillator has a phase noise of around -82 dBc/Hz at 1 MHz offset at 250 GHz carrier frequency with 0 V back gate bias. The phase noise slightly deteriorates with increase in V_{bg} and becomes nearly -76 dBc/Hz at -1 V back gate bias (see Fig. 7). For network-on-chip applications (see below) where there is negligible interference of undesired signals and a simple OOK modulation is used, the mediocre phase-noise performance of the proposed oscillator at 250 GHz can be tolerated. However, improvement of phase noise via additional circuit elements and higher transconductance appears to be necessary for phase-critical modulation schemes such as PSK and QAM.

IV. Application Example: Wireless On-Chip Networks

The sub-THz push-push oscillator proposed here is the continuation of the mm-wave Colpitts oscillator reported in [6]. Both of these designs are intended for use in the novel and unique Optical-Wireless NoC (OWN) architecture for kilo-core computing that utilizes both optical and wireless interconnects [10]. The dual use of the optical and wireless technology allows OWN to maximize the efficiency of lasers (as these are always on), reduce latency (while waiting for tokens, time slots for broadcasting) and reduce insertion losses

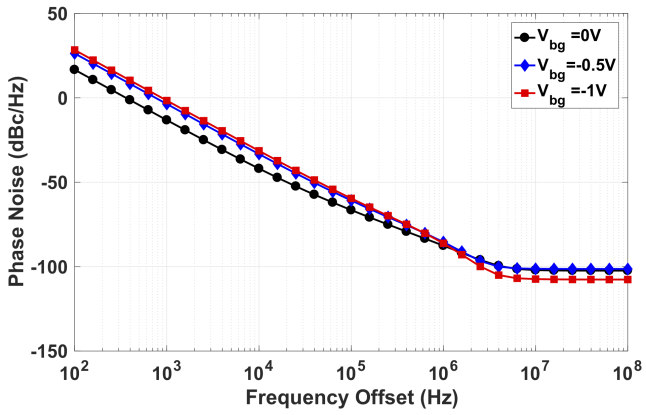

Fig. 7. The phase noise at the center frequency of 250 GHz.

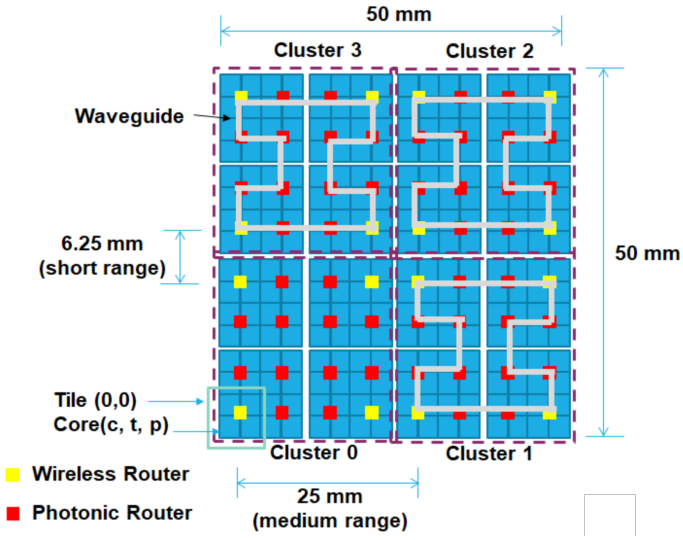

Fig. 8. 256-Core OWN architecture that combines optical and wireless routers. Wireless routers communicate with each other in uniquely assigned bands [10] using an OOK transmitter with tunable amplitude power.

(shorter waveguides). Wireless technology is utilized to interconnect the clusters wherein the hop count is reduced and additional bandwidth can be dynamically and economically allocated. The combined impact is that we can build kilo-core architecture using a maximum of three-hops for any-to-any core communication. The results indicate that OWN consumes 30.36% less energy, and improves throughput by 8% over wireless architectures and obtains 35.5% less area than purely optical architectures [10].

The sub-THz push-push oscillator implemented here can be employed in the design of the OOK transmitters which will be subsequently used in the OWN architecture. At least 16 such transmitters tuned to various frequencies from 30 to 400 GHz is envisaged. In the final design, the proposed push-push oscillator will be coupled directly to the antenna, reducing both area and power associated with power amplifiers. Obviously smaller FinFETs and improved passives with lower parasitics is needed to achieve these objectives.

Another useful feature of the proposed push-push VCO for the OWN architecture is the presence of high-order harmonics that can be utilized for high frequency oscillators. In the present topology, such harmonics can be combined to result in 2^{nd} and even higher order harmonic oscillators in a relatively efficient and straightforward manner. Since wireless links require carriers up to 400 GHz range, push-push oscillators can be a viable option to build these sub-THz links for OWN.

V. Conclusion

This paper demonstrates the several merits of the novel BSIM-IMG FinFET model in the design of the compact and efficient push-push oscillator operating at 250 GHz. In order to reduce the overall RC time constant and achieve sub-THz frequency, external capacitors have been eliminated in favor of intrinsic higher FinFET parasitics in the design of the oscillator circuit. Advantages of the use of FinFETs are highlighted, which includes more lenient oscillation criterion, smaller overall area, lower power dissipation and broader tuning range. To improve accuracy of the simulations a full-3D electron-magnetic model of the inductors are employed and incorporated into the circuit simulation. It has been validated that independent-gate FinFETs can be used to build tunable sub-THz oscillators in an efficient manner, which is a requirement to build wide-band on-chip wireless routers in kilo-core computing. Although the proposed design is not verified experimentally, the use of experimentally-tuned BSIM-IMG FinFET model and professional EDA tools augmented with accurate E-M modeling provide confidence in the proposed oscillator design.

Acknowledgment

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