Sustainability in Network-on-Chips by Exploring Heterogeneity in Emerging Technologies

Avinash Karanth[®], Savas Kaya[®], Ashif Sikder, Daniel Carbaugh, Soumyasanta Laha, Dominic DiTomaso, Ahmed Louri, Hao Xin, and Junqiang Wu[®]

Abstract—With the scaling of technology, the computing industry is experiencing a shift from multi-core to many-core architectures. However, traditional metallic-based on-chip interconnects may not scale to support many-core architectures due to high power dissipation, and increased communication latency. Attention has recently shifted to emerging technologies such as silicon-photonics and wireless interconnects to implement future on-chip communications. Although emerging technologies show promising results for power-efficient, low-latency, and scalable on-chip interconnects, the use of single technology may not be sufficient to scale future architectures. In this paper, we extend the heterogeneous architecture Optical-Wireless Network-on-Chip (OWN [1]) to Reconfigurable Optical-Wireless Network-on-Chip (R-OWN) by introducing run-time reconfigurable wireless channels. Like OWN, R-OWN is designed such that one-hop photonic interconnect is used up to 64 cores (called a cluster) and communication beyond a cluster is one-hop wireless to limit the network diameter to a maximum of three hops. The photonic bandwidth is efficiently shared using time division multiplexing (TDM) while the wireless bandwidth is shared using frequency division multiplexing (FDM). By exploiting the heterogeneity of two emerging technologies, we reduce the energy/bit, improve performance via reconfiguration, and thereby improve the sustainability of NoCs and CMPs. We propose a preliminary assessment of implementing heterogeneous technologies with the router microarchitecture. Further, we also discuss the design of horn antenna for implementing the wireless channels. Our results indicate that R-OWN improves the performance (throughput and latency) by 15 percent when compared to OWN while consuming 7 percent more energy than OWN. Further, OWN and R-OWN improve energy-efficiency by 54-61 percent when compared to WCube and CMesh architectures, respectively. It should be noted that both OWN and R-OWN require less area than state-of-the-art wired, wireless, and optical on-chip networks.

Index Terms—Network-on-chips, wireless, photonics, reconfiguration, transceivers, antennas

1 INTRODUCTION

THE International Technology Roadmap for Semiconductors (ITRS) predicts that complementary metal-oxide semiconductor (CMOS) feature sizes will shrink to 11 nm by 2020 [2]. As a result, billions of transistors will allow computer architects to accommodate hundreds or even thousands of cores on a single chip without altering the current chip dimensions [3]. However, global wire delays and energy costs do not scale down with CMOS technology. Therefore, based on ITRS predictions, traditional metallic interconnects may not be able to support many-core chip multiprocessors (CMPs) due to energy and performance limitations. As energy consumption due to both static and

- A. Karanth, S. Kaya, A. Sikder, D. Carbaugh, S. Laha, and D. DiTomaso are with the Department of Electrical Engineering and Computer Science, Ohio University, Athens, OH 43110. E-mail: {karanth, kaya, ms047194, dc136407, sl922608, dd292006]@ohio.edu.
- A. Louri is with the Department of Electrical and Computer Engineering, George Washington University, Washington, DC 20052.
 E-mail: louri@gwu.edu.
- H. Xin and J. Wu are with the Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ 85721.
 E-mail: {hxin, jqwu}@email.arizona.edu.

Manuscript received 21 Mar. 2017; revised 21 Mar. 2018; accepted 29 Mar. 2018. Date of publication 31 July 2018; date of current version 5 Sept. 2019. (Corresponding author: Avinash Karanth.) Recommended for acceptance by R. G. Melhem. For information on obtaining reprints of this article, please send e-mail to: reprints@ieee.org, and reference the Digital Object Identifier below.

Digital Object Identifier no. 10.1109/TSUSC.2018.2861362

dynamic CMOS components continues to grow, a sustainable solution that is both energy-efficient and high-performance is required. Disruptive technologies such as wireless and photonic interconnects have great potential to provide a sustainable solution for the energy crisis facing multicore architecture. Consequently, emerging technologies can deliver adequate bandwidth within the power budget for network-on-chips (NoCs) in future CMPs.

Photonic interconnects offer several advantages such as low energy consumption (~0.25 pJ/bit), reduced link latency (~ps), increased bandwidth-density (~40 Gbps) via wavelength division multiplexing (WDM) and CMOS compatibility-all of which makes silicon photonics a suitable technology for on-chip communications [4], [5], [6], [7], [8]. However, photonic crossbar-based architectures such as Corona [4], decomposed crossbar based architectures such as Firefly [5] and 3D-NoC [8] suffer from scalability issues for large core counts due to significant area and power overhead. For example, a 64×64 crossbar using photonics will require 448 modulators, 7 waveguides and 28,224 photodetectors using single-writer multiple-reader (SWMR). If we scale to 1024×1024 , then we will need approximately 7,168 modulators, 112 waveguides, and 7.3 million photodetectors which is prohibitive and not easily scalable to mitigate thermal variations. Additionally, large photonic crossbars suffer from high insertion losses due to long snakelike waveguides and crossovers (splitters). An alternate choice

^{2377-3782 © 2018} IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.



Fig. 1. Shows the design where we compare electrical link with one repeater, several repeaters, photonic link, and wireless link. Electrical and photonic numbers were obtained from DSENT.

is to reduce the crossbar size, however the penalty will be increased number of hops which negatively impacts energy-efficiency and network latency.

Radio-frequency (RF)/wireless NoCs has the advantages of CMOS compatibility, distance-independent communication, and omni-directional communication-all of which can reduce the energy consumption by decreasing hop count [3], [9]. Therefore, wireless technology can easily implement unicast, multicast and broadcast communications as it does not require physical channels such as waveguides or wires. While frequency division multiplexing (FDM), time division multiplexing (TDM), and space division multiplexing (SDM) can be effectively combined to increase the overall wireless bandwidth, mmwave transceivers at 60 GHz center frequency offer fewer channels that can be implemented in current technology while larger bandwidth transceivers operating at 100-300 GHz is more challenging to implement [10]. So, wireless architectures are designed as a two-tier hybrid architecture where wireless is used to connect subnets (a group of cores) and each subnet is connected using wired mesh or fully connected networks [3], [9], [11].

While photonic interconnects offer several advantages such as energy-efficiency and high bandwidth, scaling to large core counts becomes prohibitively expensive (hardware resources, insertion losses). Similarly, omnidirectional wireless enables ease of communication, limited frequency spectrum and higher energy/bit are the limitations of wireless technology. Therefore, we propose to exploit the advantages of the emerging technologies while circumventing their disadvantages. Fig. 1 shows the energy consumed for different technologies (wireless, wired and photonic) for varying distances. Wired (one repeater and several repeaters) and photonic numbers are reported from DSENT in 45 nm where as wireless numbers are projected values (see Section 5). The energy/bit varies for photonic link marginally changes with distance. For 1 mm link and 128 bit flit width, the photonic link consumes 0.165 pJ/bit where as for 20 mm, the photonic link consumes 0.171 pJ/bit [12]. From the Fig. 1, we can see that photonics is advantageous beyond 4 mm and wireless is beyond 10 mm. While Fig. 1 shows wired technology to be energy-efficient for distances lesser than 4 mm and could be considered more energy-efficient than photonics at such short distances, as packets travel from source to destination, additional router power will be consumed at each intermediate router which will make wired technology less favorable. From this analysis, we propose to utilize photonic technology for short distances by connecting few cores and utilize wireless technology for long distance irregular communication. By exploiting the heterogeneity of two emerging technologies, we propose to reduce the energy/bit, improve performance and overall power consumption of the network, thereby improving the sustainability of NoCs and CMPs.

In our prior work [1], we proposed Optical-Wireless Network-on-Chip (OWN) architecture for kilo-core CMPs. OWN uses decomposed photonic crossbar to communicate with a group of cores (called cluster) and dedicated wireless links to connect the clusters. In this work, we extend OWN to Reconfigurable Optical-Wireless Network-on-Chip (R-OWN) wherein we design wireless links that can be reconfigured at runtime to take advantage of diverse communication patterns. As most on-chip applications have communication patterns that are largely unpredictable in time and space, an interconnect which can dynamically reallocate bandwidth during run time could alleviate an over-utilized channel by reallocating bandwidth from an under-utilized channel. While photonics and wireless could both be ideal candidates for re-allocating bandwidth in NoC, in this work, we have considered wireless interconnects for reallocating bandwidth due to the lack of wires and wide frequency spectrum. Moreover, we analyze the implementation complexity of the router microarchitecture using wireless and photonic transceivers and characterize antenna design for our architecture. Our results indicate that R-OWN improves the performance (throughput and latency) by 15 percent when compared to OWN while consuming 7 percent more energy than OWN. Further, OWN and R-OWN improve energy-efficiency by 54-61 percent when compared to WCube and CMesh architectures respectively. Our area results indicate that both OWN and R-OWN require less area than state-of-the-art wired, wireless and optical on-chip networks. The major contributions of this work are as follows:

- *Extending R-OWN:* We extend R-OWN by refining the inter-core communication and deadlock freedom while implementing wireless bandwidth reallocation based on application demands. We provide details on architecture, routing and reconfiguration in R-OWN design.
- *Wireless Transceivers:* We discuss the feasibility of implementing R-OWN architecture that includes photonics and wireless technologies integrated with CMOS. We discuss advanced transceiver technologies such as SiGe and BiCMOS for scaling the wireless bandwidth for on-chip interconnects.
- *Wireless Antennas:* We also show the feasibility of implementing HORN antennas for R-OWN architecture.
- *Performance:* Our results indicate that R-OWN improves the performance (throughput and latency) by 15 percent when compared to OWN while consuming 7 percent more energy than OWN. Further,

OWN and R-OWN improve energy-efficiency by 54-61 percent when compared to WCube and CMesh architectures respectively.

The paper is organized as follows: in Section 2, we discuss related work; in Section 3, we describe the sustainability in NoCs; in Section 4, we describe the proposed OWN and R-OWN architecture, communication and deadlock freedom; in Section 5, we describe the feasibility study with wireless and photonic transceivers and antennas; in Section 6, we show the performance evaluation; and in Section 7, we conclude the paper.

2 RELATED WORK

In this section, we briefly discuss prior work relevant to our proposed architecture. One of the earliest wireless NoC architecture that scaled to 1,024 cores is WCube [3]. WCube extends the CMesh architecture using wireless routers for every group of 16 routers, and wireless is used only for long distance communication which is multi-hop in nature. The frequency spectrum of operation is 100-500 GHz and an energy of 4.5 pJ/bit is proposed for wireless link. Although, WCube is scalable by increasing the number of groups and without quadratically increasing the network diameter, it creates hot-spots at the group wireless router and the frequency spectrum cannot be reused due to the nature of frequency sharing among different groups. Other wireless architectures [9], [13], [14] uses wired technology for smaller sets of routers and wireless for longer distance using on-off keying (OOK) modulation. Wireless channels are shared using tokens by combining time division multiplexing and frequency division multiplexing. iWISE is extended to A-WiNoC [15] by providing adaptability in wireless channels in order to reduce network contention. Other graphene based wireless interconnects have also been proposed for on-chip interconnects to improve energy-efficiency [16].

In more recent work, several of the research have focused on saving power or performance using voltage/frequency scaling or synchronization that are orthogonal to the proposed research. For example, some of the recent research have proposed to improve the latency and energy dissipation using millimeter-wave small-world wireless NoC (mSWNoC) that prunes dynamic voltage and frequency levels (DVFS) that improves the energy-delay product [17]. Static and dynamic power of NoCs is reduced with wireless technology in [14]. Taking advantage of the wireless LAN behavior, some of the researchers have proposed to use carrier sense multiple access with collision detection (CSMA-CD) for improving synchronization in cache coherent multicore architectures [18]. Other wireless designs have targeted accessing off-chip memory and multicores to improve power and performance [19], [20]. While several of these wireless designs exploit architectural properties such as voltage scaling, synchronization or off-chip access these are orthogonal to the proposed research since in this research, we target scaling to kilocores usign heterogeneous emerging technologies.

Photonic NoCs are drawing considerable interest due to their inherent energy and bandwidth advantages. Early NoCs mostly use global photonic crossbar and wavelength division multiplexing [4], [5], [21]. Corona [4] proposes an optical ringcrossbar network using the broadcasting capability of the photonic links. It uses single-writer-multiple-reader to provide one hop optical communication between any two cores and each router is connected to a memory controller using optical link. It uses off-chip laser source and dense wavelength division multiplexing (DWDM). However, it requires several waveguides and consumes high power as a portion of the wavelength is peeled off by every router on the path. Firefly reduces the optical crossbar costs by utilizing electrical mesh while 3D-NoC reduces the cost utilizing decomposed crossbars. Clearly, crossbar-based architectures using photonic technology face scalability challenges.

As compared to several proposed architectures that use emerging technologies, R-OWN uniquely combines both photonic and wireless technologies with reconfigurability within the same architecture. The difference between R-OWN and other photonic crossbars is that R-OWN uses photonic crossbars for local communication and uses wireless for global communication. Moreover, we also analyze the implementation complexity and antenna design for R-OWN architecture.

3 SUSTAINABILITY IN NOCS

As computer systems are composed of cores, memories and interconnects, improving sustainability implies that the system needs to become energy-efficient and reliable in all aspects of computation, storage and communication. In this paper, we focus on the interconnect and propose techniques to reduce the power consumption of the network, and improve the lifetime reliability of the chip. Voltage scaling, power-gating and more recently, near threshold voltage (NTV) has been proposed to reduce the power consumption (dynamic and static power) of the NoC. Decreased power consumption leads to reduced peak temperatures which leads to reduction in hard faults, and improves the reliability of NoCs. However, voltage scaling increases the NoC susceptibility to timing errors since it reduces voltage margins and increases the probability of errors. If voltage scaling is not employed, then temperature increases which impacts aging of circuits and increases hard faults in the network. Therefore, while traditional techniques improves sustainability of NoCs, there are design trade-offs between reliability, temperature and voltage scaling that affect reliability.

In this paper, we leverage emerging technologies such as photonics and wireless interconnects to reduce the power consumption. Our goal is to improve the lifetime reliability of the NoC by reducing the power density by exploiting the advantages of emerging technologies. To achieve high datarates required by wireless technology, we propose to employ advanced transceiver technology built with SiGe and BiCMOS. While the newer technology will impose additional fabrication costs, we believe that these additional costs will be mitigated by improved reliability for inter-core communication. In the next sections, we describe the proposed architecture and performance evaluation.

4 PROPOSED R-OWN ARCHITECTURE

In this section, first, we briefly explain our 64-core and 256core OWN architecture [1]. Second, we describe the design of R-OWN for 256 cores and describe routing mechanisms. Third, we analyze deadlock situations especially when



Fig. 2. Shows the 64-Core OWN architecture, connected by 16×16 optical crossbar with inset showing the proposed wireless router (top) and optical router (bottom). WR1 and WR2 are connected with other wireless routers.

packets flow from multiple domains (optics to wireless) and describe a deadlock-free routing methodology.

4.1 64-Core OWN Architecture: Cluster

The OWN architecture is a tile-based architecture with each tile consisting of four processing cores and their private L1 instruction and data caches, a shared L2 cache and a network interface or router. Each tile is located within a *cluster*, which consists of 16 such tiles (64 cores) as shown in Fig. 2. The tiles inside a cluster are represented by two coordinates (r, c) where r is the number of the tile or the router and c identifies one of the four cores in that tile. These tiles are connected by a 16×16 optical crossbar which is the snake-like optical waveguide and takes one hop for core-to-core communication, as shown in Fig. 2. We use multiple-write-single-read (MWSR) scheme with arbitration wherein each tile is assigned dedicated wavelength(s) to receive messages from the remaining 15 tiles. The tradeoff in using MWSR is increased latency since each router must wait to grab the token before writing to a specific channel. As there are 16 routers inside the cluster and communication between the routers require only one hop, we argue that this latency will not dramatically affect the performance. So, any one of the 15 tiles of 64-core OWN architecture can write to the other tiles such that all the 16 tiles can read at the same time in their assigned wavelength(s). Thus, each cluster requires two waveguides. For example, a core in router 2 wants to send a packet to router 11. Router 2 will wait for the token to modulate the wavelength(s) assigned to router 11. Having the token, router 2 will modulate the appropriate wavelength(s) to router 11 which is shown as yellow in Fig. 2. In addition, an arbitration waveguide is used to arbitrate between multiple routers wanting to transmit to the same receiver, so that signal integrity is maintained.

4.2 256-Core OWN Architecture: Group

As mentioned, 16 tiles form a cluster, and four clusters form 256-core OWN architecture which is shown in Fig. 3. Intra-cluster communication is implemented using optical interconnects while inter-cluster communication is facilitated using wireless interconnects. Since we have four clusters, twelve (${}^{4}P_{2}$) unidirectional channels are required to provide cluster-to-cluster wireless communication. Unique pairs of frequency channels are assigned for communication between each pair of clusters. So, each cluster needs three frequency channels to talk to the rest of the clusters (horizontal, vertical, and diagonal cluster). As a result, each cluster contains three transmitters to send packets to the horizontal, vertical and diagonal cluster. Similarly, each cluster has three receivers tuned at the transmitter frequencies of other clusters to receive packets. Therefore, each cluster will have three



Fig. 3. 256-Core OWN architecture. Routers with the same color communicate with each other and Fxy represents a wireless channel to send packets from cluster x to cluster y. For example, Routers H0 and H1 communicate with each other over frequency channel F01 and F10, respectively, while routers V1 and V3 communicate with each other over frequency channel F13 and F31, respectively.



Fig. 4. Left: Structure of a cluster in R-OWN architecture. Right: Structure of a wireless router in R-OWN with transmitters, receivers, counters, and local arbiter.

transceivers: one for horizontal, one for vertical and one for diagonal cluster communication. The bandwidth of the wireless channels are determined by dividing the total bandwidth with the number of channels required.

Three of the four corner routers of each cluster (Fig. 2) is chosen for the on-chip wireless communication. The corner routers are chosen to provide maximum separation between transceivers operating at different frequencies to minimize inter-channel interference. The innermost corner routers (marked with red box in Fig. 3) of 256-core OWN is not used for the convenience of scaling to 1,024-core OWN [1]. For example, a core of the bottom left cluster wants to send a packet to a core at the top right cluster which requires intercluster transition. Since the transmitter of router D0 at the source cluster is tuned with the receiver of router D3 at the destination cluster, router corresponding to the source core (if not D0) will wait for the token to write to the optical link associated with the router D0. After receiving the packet, D0 will send the packet to D3 using the wireless link, F03 and D3 will send packet to the destination router modulating the corresponding optical link. Complete routing mechanism is discussed later.

4.3 Proposed Reconfigurable-OWN (R-OWN)

OWN 256-core architecture is extended to R-OWN architecture by incorporating reconfigurability in the network. Each cluster of R-OWN is assigned an adaptive wireless channel in addition to the fixed wireless channels present in the OWN 256-core network. The trade-off is reduced bandwidth for more adaptability with network traffic. So, each wireless router of a cluster contains a transmitter tuned to the adaptive wireless channel frequency assigned to that cluster. However, only one of them can operate for a period of time to maintain signal integrity which is determined by an arbiter. Each wireless router of a cluster contains a receiver to accept packet from other clusters. For this purpose, the receivers are tuned at the adaptive wireless channel frequency assigned to other clusters in such a way that only one wireless router can accept packet from a certain cluster. The structure of a cluster of R-OWN is shown in Fig. 4 (top). It shows that router H0, V0, and D0, each contains a transmitter T0 tuned at the adaptive wireless channel frequency of cluster 0. Router H0 has receiver R1 tuned at the adaptive wireless channel frequency of cluster 1, T1. Similarly, receiver R2 and R3 of V0 and D0 are tuned to adaptive wireless channel frequency T2 and T3 of cluster 2 and 3 respectively.

Algorithm 1 shows the proposed wireless bandwidth reconfiguration algorithm. Since we calculate the maximum

usage, there could be scenarios when the usage is the same for different contending wireless routers. In such cases, the adaptive wireless channel will be allocated to the router with the lower ID. The link usage is only calculated on the outgoing links. The adaptive wireless channel of each cluster is reconfigured after reconfiguration window (set to 100 cycles in our simulation) depending on the number of packets sent to the other clusters. The reconfiguration window size of 100 cycles was assumed from prior work where we performed similar bandwidth reallocation [8]. With smaller window size, we observed fluctuations in wireless bandwidth allocation and with larger window size, we did not observe any gains in performance. The control messages are exchanged using data packets on the wireless channels. After every 100 cycle, the wireless routers of each cluster send their corresponding wireless link utilization to the local arbiter of that cluster. The local arbiter determines the destination cluster of the adaptive wireless link for the next 100 cycle based on the maximum link utilization. So, each wireless router needs a counter to keep track of the wireless link traversals and each cluster need an arbiter to configure adaptive wireless link. This is shown in Fig. 4. We determine the maximum size of the counter by dividing the time difference between reconfiguration time frame and one router pipeline with the wireless link traversal time. When a router has the right to use the adaptive wireless channel, it has two wireless links connected to the destination cluster. We chose to send packets to the adaptive and fixed wireless links alternatively in order to minimize contention. Otherwise, we use the dedicated wireless link to communicate with the other cluster. For example, at the end of a reconfiguration time frame, router H0, V0, and D0 will send the number of traversals for wireless link F01, F02, and F03 respectively. Local arbiter LA0 will find the maximum wireless link utilization and assign accordingly. If router H0 is assigned the adaptive wireless link F0 for the next time frame and packet p1 is destined for cluster 1, H0 will send p1 using F01. H0 will send the next packet, say p2 destined for cluster 1 via F0.

Algorithm 1. Reconfigurable-Wireless Algorithm				
Step1	Wait for the end of reconfiguration time frame, $\rm R_{tf}~(\approx 100~cycle)$			
Step2	At the end of R_{tf} , Local arbiter (LA _i) requests the wireless routers of that cluster for their corresponding wireless link usage (WL _{iH} , WL _{iV} , WL _{iD}) where i is the cluster number and H is horizontal, V is vertical, and D is diagonal wireless link			
Step3	Each wireless router of cluster i sends their wireless link usage for the last $R_{\rm tf}$ to ${\rm LA}_i$ and r esets the counter to zero			
Step4	$\rm LA_i$ finds the maximum of $[\rm WL_{iH}, \rm WL_{iV}, \rm WL_{iD}]$ and sends a control packet to all the wireless routers of that cluster			
Step5	Accepting the packet, each wireless router either turn-on or turn-off their adaptive transmitter			
Step6 Step7	Wireless router that has turned-on the adaptive transmitter uses the adaptive and fixed wireless transmitters. Go to Step1			

In summary, each wireless router of a cluster contains an adaptive transmitter, T_i where $0 \le i \le cs$, a receiver R_i



Fig. 5. Communication mechanism for 256-core (a) OWN and (b) R-OWN. The uniform dotted line represents fixed wireless link, nonuniform dotted line represents adaptive wireless link, and the solid line represents optical link. Routers of the same letter talk to each other.

tuned at the adaptive transmitter of other cluster, T_j where $0 \leq j \leq cs$ and $i \neq j$, a fixed transceiver to communicate with the other clusters similar to OWN and a counter to keep track of the wireless link traversals. In addition to these, each cluster contains a local arbiter.

4.4 Routing Mechanism: 256-Core OWN and R-OWN

There are four clusters in 256-core OWN where each cluster contains 64 cores. Each core is represented by a 3-digit coordinate with *cluster, router*, and *core* number. It is represented as (cs, r, c) where *cs* is cluster, *r* is router, and *c* is core number. Thus, the total number of cores in OWN or R-OWN is $cs \times r \times c$, where $0 \le cs \le 3$, $0 \le r \le 15$ and $0 \le c \le 3$. Since each router contains four cores, we drop the core index when identifying a router. In the following sections we will describe the routing mechanism of OWN and R-OWN in detail which are very similar. However, R-OWN has more channels than OWN but less bandwidth per channel with adaptivity that makes the difference in routing.

4.4.1 256-Core OWN Communication

Consider Fig. 5a for the detailed communication pattern of 256-core OWN. For example, core (0, 0, 0) is in cluster 0 (bottom-left), and at the first tile (router 0). If it wants to send a packet to core (1, 7, 3) which is in cluster 1 (bottom-right), then it is an inter-cluster communication. First, core (0, 0, 0)will send the packet to router 0 where the packet will wait for the token to modulate the wavelengths assigned to the right-most corner router (0,3) (shown as H). Once the packet arrives at the wireless router (0, 3), it will send the packet using horizontal wireless link (F01) to the wireless router (1, 3) of cluster 1 (also shown as H). Then router (1, 3) will forward the packet to the destination router (1, 7) where core (1, 7, 3) is connected over the optical link when it has the token to write to the wavelengths assigned to (1, 7). This will require three hops-one optical, one wireless and one optical. Let's consider another inter-cluster communication where the clusters are along the diagonal. Say, the source core is (1, 4, 3) and destination core is (2, 15, 3). The source core (1, 4, 3) will insert the packet to the router (1, 4). This will send the packet to wireless router (1, 0) using optical link after receiving the token. It will then use the wireless channel F12 to transmit the packet to the wireless router (2, 12). It will then send the packet optically to the destination router (2, 15) where it will be ejected from the network. The whole transmission will take three hops (optical-wirelessoptical). Similarly, cores (1, 13, 2) to (3, 0, 3) use vertical wireless link (F13) to reach the destination which is shown in Fig. 5a. So, the minimum hop count is one (optical, intracluster) and the maximum hop count is three (optical-wireless-optical, inter-cluster) for 256-core OWN architecture. The lower diameter of OWN contributes to lower energy and latency. From Fig. 4, the router shows that the core is directly connected to wireless or optical transceiver. If intratile communication is considered, there is only traversal over the crossbar of the local router. the router shows that the core is directly connected to wireless or optical transceiver. If intra-tile communication is considered, there is only traversal over the crossbar of the local router. While two optical hops are required, OWN architecture is more scalable than a pure-photonic architecture since wireless links provide additional flexibility by connecting different photonic domains. For inter-cluster communication, the two fixed antennas send packets back and forth. This is when they will inform the transmitter of the amount of free VCs in the incoming buffer. This ensures that there is no overflow of packets between wireless transmitters.

4.4.2 256-Core R-OWN Communication

Consider the R-OWN communication shown in Fig. 5b. The basic routing mechanism of R-OWN is similar to OWN. The modification is the use of adaptive wireless links. For example, core (0, 0, 0) and (0, 4, 2) both want to send packet to core (1, 7, 3) and router (0, 3) possess the adaptive wireless link of cluster 0. That is the adaptive wireless link, F0 is connected to cluster 1 at this point of time. Both the cores will need to send packet to the wireless router (0, 3) for intercluster wireless transmission. By modulating the wavelengths associated with router (0, 3), one of the cores will send the packet first and then the next one. Assume both the packets are now sitting at the buffer of router (0, 3). Since two wireless links (one fixed, F01 and one adaptive, F0) are now connected to the wireless router (1, 3) of cluster 1, these two packets will be sent concurrently using F01 and F0. At the same reconfiguration time frame, for example two cores of cluster 0 want to send packet to cluster 2 which requires the use of vertical wireless link (F02). Since only one wireless link is connected to cluster 2 from cluster 0, both the packets will contend for F02 at the router (0, 12) and whichever wins the arbitration will transmit. On the other hand, say the adaptive wireless link of cluster 1 (F1) is pointing to cluster 3 as shown in Fig. 5b. Hence, cores (1, 13, 2) and (1, 11, 1) both will be able to send packet at the same time using fixed wireless channel, F13 and adaptive wireless channel, F1 to their destination cluster 3 once they reach the wireless router (1, 12). This is possible, because each cluster has its own adaptive wireless link and it is configured based on the outgoing traffic from that cluster only. Now, consider core (1, 13, 2) send the packet first to destination (3, 7, 1) using wireless link F13. Then if core (1, 11, 1)wants to talk to core (3, 0, 3), router (1, 12) will assign the wireless channel F1 instead of F13 as it was used last time. So, when a wireless router do not have access to the adaptive wireless link, it follows the same routing procedure as OWN and when a wireless router retain the right of the



Fig. 6. (a) Possible deadlock scenarios in a 256-core OWN, (b) routing path and channel dependency for the deadlock-prone network, and (c) routing path and channel dependency for the deadlock-free network. H0, D0, H1, V1, V3, and D3 represent wireless router. Solid lines represent optical link (marked as O_x) where dotted lines represent wireless link (marked as W_x). Transmission paths of inter-cluster packet A, B, and C are shown in yellow, red, and dark blue, respectively.

adaptive wireless link, it either chooses one of the wireless links (fixed and adaptive) or uses both.

4.5 Deadlock Free Routing

There are two types of communication in OWN architecture: intra-cluster (optical) and inter-cluster (wireless). Either intra or inter-cluster communication in isolation does not create deadlocks, however when these two phases of communication are required, then deadlocks are likely to occur. In Fig. 6a communication path of three packets are shown. Packet A originates at router D0, takes the optical link (O_1) to the wireless router H0, travels through the wireless link (W_1) to arrive at router H1 and then reaches the destination router V1 via optical link (O_2) where it exits the network. Similarly, travel path of packet B is: H1-optical link (O2)-V1-wireless link (W2)-V3-optical link (O₃)-D3 and packet C is: V3-optical link (O_3) -D3-wireless link (W_3) -D0-optical link (O_1) -H0. All the packets require three hops to reach their respective destination router from the source router. The channel dependency graph for this network is shown in Fig. 6b. It can be seen that a circular channel dependency exists in the network due to the simultaneous transmission of packet A, B, and C which can be written as: $O_1 -> W_1 -> O_2 -> W_2 -> O_3 -> W_3 -> O_1$.

There are different types of deadlock avoidance techniques. In this work we have provided separate paths for intra-cluster and inter-cluster communications to avoid deadlocks. To break this circular dependency shown in Fig. 6b, we introduce new optical links (O_4, O_5, O_6) with usage restriction. Since we are using MWSR, we assign new wavelengths to the wireless routers where routers that do not have necessary wireless link to perform inter-cluster communication can write. However, on the destination cluster, packets are sent through the optical links that were present before. So the travel paths for packet A, B, and C are D0-optical link (O₄)-H0-wireless link (W₁)-H1-optical link (O_2) -V1, H1-optical link (O_5) -V1-wireless link (W_2) -V3optical link (O₃)-D3 and V3-optical link (O₆)-D3-wireless link (W_3) -D0-optical link (O_1) -H0 respectively. Therefore, the new optical links (O_4 , O_5 , and O_6) are used only by the intercluster packets to travel from the source router to the wireless router and the corresponding channel dependency is shown in Fig. 6c. As can be seen, the proposed network is deadlock free which ensures all packet delivery. The trade-off is increased area and power for more links. However, we can argue that since an optical waveguide contains 64 wavelengths, we can use the unused wavelengths without incurring any area or power overhead.

Deadlock Freedom per Cluster. To generalize, consider cluster 0 with three static wireless routers V_0 , D_0 and H_0 . Now traffic can flow into and out of the cluster through only the wireless routers i.e., cluster 1 can communicate with cluster 0 using $H_1 -> H_0$ and similarly, cluster 0 can communicate with cluster 1 using $H_0 -> H_1$. Therefore, to break any cycles, we need to create more optical links between the wireless routers. Considering all intra-cluster communication due to intercluster traffic, $V_0 -> D_0$, $V_0 -> H_0$, $D_0 -> H_0$, $D_0 -> V_0$, $H_0 - > V_0$ and $H_0 - > D_0$ a total of 6 extra optical channels are required to break deadlocks since we are using MWSR design. When the wireless channel is used for reconfiguration, the deadlock avoidance simplifies since there are two wireless channels instead of one wireless channel and it can break the deadlock. Therefore, including a wireless channel that can be reconfigured simplifies the deadlock process.

When the wireless channel is used for reconfiguration, the deadlock configuration simplifies since there are two wireless channels instead of one wireless channel and it can break the deadlock. Therefore, including a wireless channel that can be reconfigured simplifies the deadlock process. We still assume that we have extra optical links and an additional wireless link when using the reconfiguration algorithm.

5 OWN IMPLEMENTATION FRAMEWORK: A FEASIBILITY STUDY

This section will identify the general implementation framework for the R-OWN architecture presented above. It is crucial to clearly point out at the outset that, at present, there is no single technology that can deliver all device, circuit and integration requirements for R-OWN. Assuming a robust on-chip wireless network that operate in 100 GHz range, not a small feat in itself, will be accessible to the designers, the crux of the matter is the implementation of photonics layer that must be assembled on the same substrate as logic and RF wireless technology. In general, it is envisaged that R-OWN must use one of the three approaches outlined in Fig. 7, where conventional silicon technology or 3-D IC integration are identified to be the most practical avenues. In the present pragmatic analysis, 'photonics front' (approach b) is



Fig. 7. Possible approaches to implement OWN interconnects. (a) Sionly approach where a dedicated photonics process must be used to build optical interconnects at the back of the wafer; or (b) the optical interconnects can be in the case of Si-only solution external laser is needed and (c) a full 3D IC integration.

considered, whereby material set and design rules of conventional CMOS interconnect technology can be used to implement a 'sub-optimal' photonic layer for optical network. However, ultimately, 3-D integration of heterogenous IC technologies (approach c) can provide more efficient and flexible path to harness optic, logic and RF performance from multiple signal domains as well as technological platforms (i.e., silicon, III- V semiconductors and printed electronics) to realize this inherently hybrid interconnect architecture. Given the stringent bandwidth and integration requirements for R-OWN architecture, it is not only reasonable to seek a heterogeneous solutions, it is actually a necessity. Not counting on the device scaling for raw performance and able to access many diverse technologies, such a heterogenous approach can lead to very unique and capable solutions that was once unthinkable [22]. Until such a holistic technology approach is viable, however, we can envision that R-OWN systems of today can be built by an elaborate integration of mm-wave Si/SiGe BiCMOS technologies and creative use of interconnect processes, as explained below.

5.1 Realization via Si/SiGe Bi-CMOS Process

Of the three approaches presented above for building R-OWN interconnects, it is believed that a Si-only approach with photonic devices implemented using a select number of metal/dielectric interconnect layers Fig. 7b is the most practical, low-cost and mature option in the short term. Neither a dedicated photonics process run on the back-side of a wafer [23], nor a full 3D integration of three complete chips [24] can compete with the cost effectiveness and relative simplicity of this approach. Accordingly, in this section, general features of a photonics front implementation for an OWN router are provided in Fig. 8, together with several circuit components to demonstrate the feasibility of \geq 100 GHz transceiver (TRX).

To avoid complexity and expenses associated with two separate process lines, we assume that all optical switching components (waveguides, modulators, and coupled-ring resonators) can be implemented at the back-end of a commercial Si/SiGe BiCMOS technology, as illustrated by several groups [25] [26] [27], [28]. It is assumed that three-metallization layers (M9-11), standard (SiO₂, Si₃N₄, SiO_xN_y) and high-K (HfO₂/ZrO₂) insulators will provide sufficient process depth to implement all necessary photonic components except the (external) laser and SiGe photodiodes on the main chip. Therefore the major electronic components for the OWN router will include the design of a low-noise optical transimpedance amplifiers (TIA) behind the photodiodes, crossbars for migration between photonic and



Fig. 8. (a) Proposed router microarchitecture that combines near-neighbor (electrical), intra-domain (optical), and inter-domain (wireless) links. Note that the actual radix will be a function of media access protocol (SWMR/MWSR) and wireless connectivity. (b) Its multi-layer implementation via diverse technology.

electrical TRX circuitry as well as the necessary mixed-signal interface for data (de)modulation using Si/SiGe BiC-MOS heterojunction bipolar transistors (HBT) with a proven potential beyond 500 GHz [28]. Since SiGe BiCMOS circuits have been extensively used for fiber communication [29] at +30 GHz data rates, it will be straightforward to adapt and simplify TIAs to ultra-low power performance and low-signal levels necessary for OWN by limiting the number of SiGe HBT gain elements and trimming the supply voltage. Another advantage of using SiGe BiCMOS circuitry is the fact that wireless TRX can also be implemented using this technology for frequencies (>180 GHz) where CMOS cannot deliver necessary signal power and bandwidth. The rest of transceiver (TRX) circuitry that operate at the baseband can be implemented using standard lowpower RF-CMOS to save power and area. The overall design target for the entire OWN router is high-efficiency (targeting $\sim 1 \text{ pJ/bit}$), minimization of crosstalk between the digital, RF and optical domains, heat management, and design of compact ultra-fast bi-directional crossbars and buffers between optical and wireless TRX blocks.

The design and optimization of wireless links is a greater challenge for the OWN architecture because of the substantial data rate ($16 \times 32 = 512$ Gbps) required, frequencies involved (\leq 600 GHz) and formidable efficiency target $(\sim 1 \text{ pJ/bit})$ to be reached. Both in terms of performance and dimensions, links delivering such level of performance is not only an unexplored territory for wireless communication, it is also beyond what current CMOS technology can deliver. Nonlinearity, frequency dependent parasitics, low gain of CMOS devices due to substrate losses and limited ft/fmax of transistor mean that multiple TRX designs in different technologies may be necessary, each optimized for the band assigned by OWN architecture. Hence at least two transceiver designs one in standard RF-CMOS and one in SiGe BiCMOS are needed, with the latter handling large frequency bands ≥180 GHz. For instance, 45 nm RF-CMOS technology is sufficient for the RF-CMOS circuitry, while the 90 nm SiGe HBTs used for optical photodetector and TIAs can be re-purposed to design high-performance power amplifiers and low-noise amplifiers in the wireless TRX



Fig. 9. (a) Two examples of ultra low-power (\leq 3 mW) and wideband (\sim 26 GHz) PA circuit and (b) a tunable oscillator designed using 55 nm BiCMOS technology. At higher frequencies, larger gain and power SiGe HBTs can provide higher gain and performance.

unit. To improve efficiency and minimize area, ultra-low voltage/power single-stage SiGe HBT LNAs [30] and frequency doubling techniques via transistor non-linear operation [31] may be necessary. Dead bands of 2-4 GHz is required to minimize inter-channel interference in the present design, as opposed to inefficient filtering techniques at 100 GHz on Si. However, in the full OWN design, once antennas and transceiver placement is completed this issue may require further analysis.

5.2 Circuit Examples

In this section, several design examples for some of the critical components of R-OWN router architecture are provided. Both space and scope of current work does not allow a more detailed study of R-OWN implementation at this time. First, we illustrate a power amplifier and oscillator example for TRX circuits, followed by a simulation example for the ring resonator crucial for optical switching in the photonics layer.

5.2.1 (Bi)CMOS Wireless Transceiver

Examples of CMOS circuits operating at 60-100 GHz bands are fairly common today, thanks to several unlicensed bands popular for indoor short-range links and vehicular radar [32], [33]. These examples constitute the baseline designs in CMOS mmwave TRX circuitry to be developed for OWN wireless links. However, OWN requires even wider bands and operation in 100s GHz. Luckily, given the persistent downscaling of CMOS devices that have resulted in transistors with 14 nm gate length, and f_t and f_{max} values already exceeding 300 GHz,

TABLE 1 Ring Resonator Simulation Results

Parameters/Results	Theoretical	Simulation	% Diff.
Resonance Peak 1 (nm)	1,534.20	1,534.90	0.023
Resonance Peak 2 (nm)	1,551.50	1,553.10	0.052
FSR (nm)	17.30	18.20	2.535
FWHM (nm)	0.88	0.82	3.529
Finesse (nm)	19.66	22.20	6.06
Q Factor (nm)	1,749.64	1,973.75	6.02
Coupling Coefficient	0.384	0.384	0.000

sub-THz CMOS circuits are not a distant possibility but an emerging platform for OWN integration [34], [35]. An example case for power amplifier and oscillator designs are made in Fig. 9, designed using 55 nm BiCMOS processes. The simple PA circuit example has 28 GHz bandwidth while the oscillator is tuned to operate for 60 GHz, which corresponds to hardware needed in the lower two bands in the proposed R-OWN interconnects. While not strictly optimized, these results show that ultra-compact and efficient RF-CMOS TRX operating \leq 180 GHz designed for OWN wireless links are well within the reach of current Si RF-CMOS technology. For higher channels where CMOS performance may be inadequate, compact and low-power amplifier and mixer circuits must be implemented using Si/SiGe HBT devices biased optimally to limit power dissipation.

5.2.2 Photonic Components

To guide photonic layer design and optimization, a ring resonator (RR) structure (the backbone of the optical links) designed using materials and thickness adapted from a standard CMOS interconnect process is shown in Table 1 and Fig. 10. Utilizing the available dielectrics (SiO_2 and Si₃N₄) at an upper metal layers as described earlier, simulations performed using the FullWave FTDT simulator was used in this 3D model design. Depending on the RR radius, proximity, height, and material choices it is possible to tune channel add/drop characteristics of the ridge waveguides and to reach a coupling factor of 0.83 and Q-factor of \sim 2000 which are sufficient for the design of SWMR/MWSR protocols defined earlier. These numbers can be further improved using more aggressive RR dimensions, material combinations and use of air (or low- κ) dielectric. The precise area and power figures must be re-calculated for the actual process to be used at the time of tape-out.



Fig. 10. Theoretical versus simulated optical intensity at the ring resonator drop-port.



Fig. 11. (a) The TEM horn antenna structure. (b) The 3D radiation pattern and (c) H plane radiation pattern of the TEM horn antenna at 160 GHz.

5.3 On-Chip Antennas

As an essential part for on chip communication, many onchip antennas have been reported [36], [37], [38], [39]. But pure inter-chip or intra-chip communication without the help of off-chip antennas is rarely realized. On-chip antennas are known as the last barrier for intra-chip communication [40]. The biggest challenge of the on-chip antenna arises from the low resistivity (thus high loss) and high dielectric constant of the thick silicon substrate [41]. When the frequency reaches millimeter wave range, the regular silicon substrate attracts and confines most of the electromagnetic energy, making the antenna radiation efficiency very low. For example, in [42], the gain of a 24 GHz dipole on a 300 um thick 10 cm silicon substrate is only measured as -8 to -10.5 dBi, which is much lower than an ideal dipole with a gain of 1.76 dBi. Another example could be a 60 GHz Yagi antenna based on 0.18-m CMOS technology [43]. The gain of this Yagi antenna is only -10 dBi due to the substrate loss. Although thinning the substrate could reduce such effect, it is not practical due to mechanical reasons. Another possible way is to add a metal layer between the antenna and the substrate as an isolation layer. Nevertheless, for antennas like dipoles, this metal layer could generate a counteractive image current very close to the original antennas thus making the radiation efficiency very low. Although artificial magnetic conductor (AMC) could reduce this effect [44], it takes considerable space and extra layers.

On chip TEM horn antenna is a promising candidate for intra-chip communications. First, TEM horn antennas have horizontally pointed radiation patterns. Thus it is suitable for intra-chip communication. Second, adding a ground plane not only reduces TEM horn antenna volume into half (see Fig. 11a), but also separates the substrate from the horn, eliminating the substrate effects on antenna and enhancing radiation efficiency. TEM horn antennas also feature wide bandwidth, which means transceivers at different frequencies can share one antenna. A very wideband on-chip TEM horn antenna with impedance bandwidth from 100 GHz to 1 THz has been realized in [45]. In this work, a TEM horn antenna has been designed with a center operating frequency of 160 GHz using the finite-element electromagnetic software Ansys HFSS. It is fed by 1.42 μ m wide microstrip



Fig. 12. (a) S_{11} of the TEM horn antenna. (b) The TEM horn antenna S_{21} comparison between the Friis equation and the simulation.

with 50 Ohm characteristic impedance on the substrate. The substrate is 0.94 μ m thick with ϵ_r = 4, which corresponds to the top layer dielectric in silicon technologies. The ground size is 10 mm by 10 mm in accordance with one cluster size. The structure of the TEM horn antenna is illustrate in Fig. 11a, where the maximum horn width a = 3.5 mm, the maximum horn height b = 1.23 mm, and the length of the horn c = 1.3 mm. Fig. 12a depicts the simulated reflection coefficient of the half horn antenna. It has impedance bandwidth from 50 GHz to higher than 250 GHz. The radiation pattern shown in Figs. 11b and 11c demonstrates that the antenna is directional with gain of 7 dB. In the H plane, the antenna gain is 2.2 dB. Channel link between two antennas separated by 15.4 mm is also simulated. The S₂₁ plot is shown in Fig. 12b. A theoretical estimation approximated in the simple Friis equation is also plotted as a reference. It is understandable that the simulated S_{21} is a bit higher than the theoretical approximation due to the near field effect.

A TEM horn has directional radiation pattern as well as wide bandwidth. But it is bulky thus become less suitable when multiple antennas are needed in limited chip area. As an alternative, vertical quarter wavelength monopole antenna which occupies a much smaller foot print is also explored. Similarly, it has horizontal radiation property and a ground plane to eliminate the impact of the silicon substrate.

An example of the on chip vertical monopole antenna is also simulated using Ansys HFSS. The antenna height is quarter wavelength at 160 GHz (468.75 m) and the diameter is 10 μ m. The ground size is 5 mm by 5 mm in accordance with a quarter cluster size. The center frequency shifts slightly to 150 GHz. The 10-dB bandwidth is about 20 GHz. The channel link of the two-antenna communication model with antenna spacing of 15.4 mm is also simulated. The simulated S₂₁ plot is shown in Fig. 13. Reasonable agreement with the theoretical estimation by Friis equation is obtained.

6 PERFORMANCE EVALUATION

To evaluate the performance of the proposed NoC architectures, we compared the 256-core architecture OWN and R-OWN with CMesh [46], WCube [3] and Opt-Xbar architectures. Opt-Xbar is a hypothetical 256-core photonic crossbar architecture with a snakelike waveguide. It contains 64 routers with concentration of four cores and uses MWSR as the arbitration technique. Each router is assigned unique wavelength(s) where all the other routers can write if they have the token. CMESH is a concentrated mesh architecture with four cores connected together with a router. WCube is also a concentrated mesh architecture, but the wireless routers are interconnected by hypercube topology [3]. There



Fig. 13. The monopole antenna $S_{\rm 21}$ comparison between the Friis equation and the simulation.

are other wired/wireless architectures [14] other than WCube which also reduce the complexity of using wireless links. However, in this paper, we have compared WCube architecture that trades-off wireless bandwidth with wired connection. We have used Dsent v. 0.91 [12] to calculate the area and power of the wired links and routers for a bulk 45 nm LVT technology. To simulate network performance for different types of synthetic traffic patterns such as uniform (UN), bit-reversal (BR), matrix transpose (MT), perfect shuffle (PS), and neighbor (NBR), we have used a cycle accurate simulator [47] keeping the clock period same for all the networks. In order for a fair comparison between different topologies, we have kept the bisection bandwidth same for all the architectures by adding appropriate delay into the network. All system level simulators allow traces to be collected up to 64 cores and beyond it has been difficult to collect traces. Since we are evaluating for 256 cores, we are using synthetic benchmarks for our evaluation. We assume we have 4 VCs with 4 buffer slots per VC for all routers. The radix includes 4 cores, 15 optical transceivers and 1 wireless transceiver. The packets are 4 flits long and with each flit 128 bit long.

6.1 Area Estimation

Area of an architecture consists of link (wired, wireless, and optical) area, and router area. As shown in Fig. 14f, Opt-Xbar acquires the highest area which is 27.63 percent higher than OWN whereas WCube, CMesh, and R-OWN acquires 27.05, 17.35, and 12.96 percent more area respectively compared to OWN. OWN, R-OWN, CMesh, and Opt-Xbar, all have 64 routers with core concentration of 4. Since OWN has lower number of input ports and the crossbar of the optical router is split into two (shown in Fig. 2), it requires less router area. This can be verified by the fact that Opt-Xbar acquires less router area than CMesh as it has large number of output ports with few input ports. WCube is built on top of CMesh and 4 wireless routers are inserted that are connected with 4 other routers. So, it requires more area than CMesh. For wireless link, we have assumed the transmitter area as 0.42 mm² and receiver area as 0.20 mm² [11]. As the number of wireless transmitters and receivers in WCube is lesser than OWN, it requires less wireless link area than OWN. Since, we extend OWN to R-OWN by implementing adaptive wireless transceivers, R-OWN requires more transceivers than OWN. Thus, it acquires higher wireless link area. It also requires slightly higher router area than OWN due to the increase in the radix of the wireless router (optical router remains the same). In this analysis we have ignored the counter and local arbiter area as they are very small. As photonic link area consists of the power, data and arbitration waveguide area, it is higher than the traditional wired link area. OWN (and thus R-OWN) requires less photonic link area than Opt-Xbar as it contains several smaller crossbar whereas Opt-Xbar contains one large crossbar.

6.2 Saturation Throughput and Latency

In this section, we discuss the latency and saturation throughput of OWN and R-OWN compared to CMesh, WCube and Opt-Xbar. WCube is an extension of CMesh



Fig. 14. Latency comparison between different networks are shown for (a) uniform traffic, (b) bit-reversal traffic, (c) matrix transpose traffic, and (d) neighbor traffic. (e) The saturation throughput of the comparing architectures with geometric mean (GM). (f) Area comparison between the compared topologies. The network load is flits/cycle/core.

Authorized licensed use limited to: The George Washington University. Downloaded on October 24,2022 at 14:03:55 UTC from IEEE Xplore. Restrictions apply.



Fig. 15. Energy per bit comparison between different topologies for various types of traffic. This energy calculation includes both leakage and dynamic components.

and takes wireless link to transmit packets requiring higher wired hops. To provide the best performance, we have optimized the distance where to take the wireless link instead of wired link during simulation. We have counted the number of wired and wireless hop required for each pair of source and destination cores, and varied the difference between them to find out the best position to take the wireless link. For fairness, we have kept the same number of VC and buffer for all the architectures. Figs. 14a and 14d shows the latency for the traffic types UN, BR, MT and NBR as a measure of number of cycles in response to a varied network load. For the uniform, bit-reversal, and matrix transpose traffic shown in Figs. 14a, 14b, and 14c respectively, OWN and R-OWN perform better than other architectures with latter being the best. This is because both OWN and R-OWN require maximum three hops to transmit to any part of the network. Since WCube uses wireless for distant source-destination pairs, it performs better than CMesh. While Opt-Xbar requires less time when the network load is low but it saturates earlier than WCube for uniform traffic. This is because, with the increase of network load the wait time for token in Opt-Xbar increases which is also true for OWN and R-OWN. However, in OWN and R-OWN, less number of routers share the crossbar. Hence, the delay increase is small. It can be also verified by observing that the zero load latency for Opt-Xbar is higher than OWN and R-OWN. For low network load, OWN and R-OWN have similar latency because the contention in the network is low and improvement due to the reconfiguration is small. However, as the load increases, R-OWN performs better than OWN as it allocates the adaptive wireless channels efficiently to the routers that are experiencing more traffic. For neighbor traffic Opt-Xbar shows the worst performance as shown in Fig. 14d. In case of neighbor traffic, the source and destination cores are close to each other and the requirement of token for every communication in Opt-Xbar increases the delay. CMesh and WCube perform better than Opt-Xbar as they do not have such delay. They also perform very similar as the wireless links in WCube are underutilized. Since wireless link utilization is low, OWN and R-OWN perform similar. However, they perform better than CMesh and WCube due to low hop requirement.

Fig. 14e shows the saturation throughput for traffic types UN, BR, MT, PS, NBR where GM is the geometric mean. As OWN and R-OWN have lowest diameter, they have highest saturation throughput for UN and MT. In case of BR, high inter-cluster communication creates contention at the wireless links and OWN has less throughput than Opt-Xbar. However, since R-OWN adapts with the load pattern, it has the highest throughput. For PS, utilization of wireless links are diverse. This causes the saturation throughput of OWN to fall as certain wireless link is over utilized where the others are underutilized. Thus, the improvement of R-OWN with respect to OWN is highest for PS. While R-OWN has 15.03 percent higher saturation throughput than OWN, OWN has 7.86, 16.58, and 20.72 percent higher saturation throughput than Opt-Xbar, WCube, and CMesh respectively.

6.3 Energy

While calculating the wired link energy consumption, we have multiplied the number of times each wired link traversed collected from the cycle accurate simulation to the corresponding wired link energy found using Dsent [12]. For wireless link, we have assumed a fixed 1 pJ for each bit transmission for both WCube and OWN. Although WCube used 4.5 pJ/bit in their paper, we think this is a technology based parameter and for fairness, all the wireless topologies should have the same wireless energy cost. During the calculation of optical link energy consumption, we have considered the worst case scenario. For OWN, R-OWN, and Opt-Xbar we have also included the power and arbitration waveguide energy consumption. We have calculated the router energy consumption per flit and taken into account the crossbar splitting of the optical router as shown in Fig. 2.

Fig. 15 shows the energy per bit comparison for UN, BR, MT, and PS traffic patterns with geometric mean. For all cases, WCube consumes equal or less wired link energy compared to CMesh as it uses wireless for distant transmission. However, WCube has lesser wireless channels than OWN and R-OWN. Hence, number of wireless link traversal and thus wireless link energy for WCube is less compared to OWN and R-OWN. As R-OWN uses more wireless channels, it consumes more wireless link energy than OWN. The difference is visible for MT and PS traffic as for these two, adaptive wireless links are well utilized which is also reflected in their saturation throughput (Fig. 14e). As photonic link energy consumption is very lower than the other technologies, it does not affect the overall energy consumption. However, OWN and R-OWN consumes order of magnitude lower energy than Opt-Xbar due to smaller crossbar size. It must be noted that while WCube uses wireless channel, it also relies on electrical wired connections and therefore, consumes more energy. As OWN and R-OWN connects directly to a cluster, the radix of the router does not significantly increase while providing extra connections in the wireless domain.

Opt-Xbar consumes lowest router energy because it has lower number of input and higher number of output ports. The first factor contributes to the lower buffer power while the second factor contributes to the lower crossbar power per flit. OWN and R-OWN consume lower router energy than CMesh and WCube. This is due to the lower hop requirement, lower number of input ports with higher number of output ports and splitting of the crossbar. However, R-OWN requires higher router energy compared to OWN due to the increase of wireless router radix. WCube has more routers with higher radix than CMesh. This is why it dissipates higher router energy compared to CMesh for BR and PS. As increasing the router radix decreases the energy consumed when compared to using multiple router traversals [48], WCube dissipates lower router energy than CMesh for UN and MT.

From the Fig. 15, we can see that more than 50 percent of the consumed energy for OWN and R-OWN dissipates as wireless link energy. This is because OWN and R-OWN use wireless for all the inter-cluster transmission whether they are neighbor or not and wireless energy per bit requirement is comparatively high. Although, WCube consume lower wireless energy than OWN and R-OWN, this off-sets the energy savings in wired link and router by making it the highest energy consumer architecture. The end result is that OWN costs 72.99 percent higher energy per bit than Opt-Xbar and 7.47, 54.4, and 61.8 percent less energy/bit than R-OWN, CMesh, and WCube respectively. Moreover, the wireless energy per bit requirement is technology dependent and as advances in technology is made, OWN and R-OWN will greatly be benefited due to the reduction of this parameter in terms of energy consumption over the other architectures compared.

7 CONCLUSIONS

In this paper, we uniquely proposed to combine two emerging technologies, namely photonics and wireless interconnects, to improve the energy/bit, scalability and overall performance of on-chip communications. Our proposed R-OWN architecture takes advantage of the adaptive frequency allocation to improve the wireless link bandwidth to achieve higher performance by adapting to application demands. By exploiting the heterogeneity of two emerging technologies, we reduce the energy/bit, improve performance and overall power consumption of the network, thereby improving the sustainability of NoCs and CMPs. With such disruptive technologies, there are several challenges for designing power-efficient transceivers and antennas. We believe that as transceiver technology and antenna design mature, heterogeneous architectures will become a reality for on-chip communication.

ACKNOWLEDGMENTS

This research was partially supported by US National Science Foundation grants CCF-1420718, CCF-1318981, CCF-1513606, CCF-1703013, CCF-1547034, CCF-1547035, CCF-1540736, and CCF-1702980. The authors thank Matthew Kennedy for the useful discussions on optical technology and reconfiguration designs.

REFERENCES

- M. I. Sikder, A. K. Kodi, M. Kennedy, S. Kaya, and A. Louri, "OWN: Optical and wireless network-on-chip for kilo-core architectures," in *Proc. IEEE 23rd Annu. Symp. High-Perform. Interconnects*, Aug. 2015, pp. 44–51.
 B. Hoefflinger, "ITRS: The international technology roadmap for
- B. Hoefflinger, "ITRS: The international technology roadmap for semiconductors," in *Chips* 2020. Berlin, Germany: Springer, 2012, pp. 161–174.
- [3] S.-B. Lee, S.-W. Tam, I. Pefkianakis, S. Lu, M. F. Chang, C. Guo, G. Reinman, C. Peng, M. Naik, L. Zhang, et al., "A scalable micro wireless interconnect structure for CMPs," in *Proc. 15th Annu. Int. Conf. Mobile Comput. Netw.*, 2009, pp. 217–228.
 [4] D. Vantrease, R. Schreiber, M. Monchiero, M. McLaren,
- [4] D. Vantrease, R. Schreiber, M. Monchiero, M. McLaren, N. P. Jouppi, M. Fiorentino, A. Davis, N. Binkert, R. G. Beausoleil, and J. H. Ahn, "Corona: System implications of emerging nanophotonic technology," ACM SIGARCH Comput. Archit. News, vol. 36, no. 3, pp. 153–164, 2008.

- [5] Y. Pan, P. Kumar, J. Kim, G. Memik, Y. Zhang, and A. Choudhary, "Firefly: Illuminating future network-on-chip with nanophotonics," ACM SIGARCH Comput. Archit. News, vol. 37, no. 3, pp. 429–440, 2009.
- ACM SIGARCH Comput. Archit. News, vol. 37, no. 3, pp. 429–440, 2009.
 [6] A. Joshi, C. Batten, Y.-J. Kwon, S. Beamer, I. Shamim, K. Asanovic, and V. Stojanovic, "Silicon-photonic clos networks for global on-chip communication," in Proc. 3rd ACM/IEEE Int. Symp. Netw.-on-Chip, 2009, pp. 124–133.
- [7] A. Krishnamoorthy, "Overview of short-reach optical interconnects: From VCSELs to silicon nanophotonics," *Hot Chips Tutorial*, San Jose, CA, Aug 22–24, 2010, Archived at https://www. hotchips.org/archives/2010s/hc22/
- [8] R. Morris, A. Kodi, and A. Louri, "Dynamic reconfiguration of 3D photonic networks-on-chip for maximizing performance and improving fault tolerance," in *Proc. 45th Annu. IEEE/ACM Int. Symp. Microarchit.*, Dec. 2012, pp. 282–293.
- Symp. Microarchit., Dec. 2012, pp. 282–293.
 [9] A. Ganguly, K. Chang, S. Deb, P. P. Pande, B. Belzer, and C. Teuscher, "Scalable hybrid wireless network-on-chip architectures for multicore systems," *IEEE Trans. Comput.*, vol. 60, no. 10, pp. 1485–1502, Oct. 2011.
- [10] D. Matolak, A. Kodi, S. Kaya, D. DiTomaso, S. Laha, and W. Rayess, "Wireless networks-on-chips: Architecture, wireless channel, and devices," *IEEE Wireless Commun.*, vol. 19, no. 5, pp. 58–65, Oct. 2012.
- [11] A. K. Kodi, M. A. I. Sikder, D. DiTomaso, S. Kaya, S. Laha, D. Matolak, and W. Rayess, "Kilo-core wireless network-on-chips (NoCs) architectures," in *Proc. 2nd Annu. Int. Conf. Nanoscale Comput. Commun.*, 2015, pp. 33:1–33:6.
- [12] C. Sun, C.-H. Chen, G. Kurian, L. Wei, J. Miller, A. Agarwal, L.-S. Peh, and V. Stojanovic, "DSENT-A tool connecting emerging photonics with electronics for opto-electronic networks-on-chip modeling," in *Proc. 6th IEEE/ACM Int. Symp. Netw. Chip*, 2012, pp. 201–210.
- [13] D. DiTomaso, A. Kodi, S. Kaya, and D. Matolak, "iWISE: Interrouter wireless scalable express channels for network-on-chips (NoCs) architecture," in *Proc. IEEE 19th Annu. Symp. High Perform. Interconnects*, 2011, pp. 11–18.
- H. K. Mondal, S. H. Gade, R. Kishore, and S. Deb, "Adaptive multi-voltage scaling in wireless NoC for high performance low power applications," in *Proc. Des. Autom. Test Eur. Conf. Exhib.*, Mar. 2016, pp. 1315–1320.
- [15] D. DiTomaso, A. Kodi, D. Matolak, S. Kaya, S. Laha, and W. Rayess, "A-WiNoC: Adaptive wireless network-on-chip architecture for chip multiprocessors," *IEEE Trans. Parallel Distrib. Syst.*, vol. 26, no. 12, pp. 3289–3302, Dec. 2015.
- [16] S. Abadal, E. Alarcn, A. Cabellos-Aparicio, M. C. Lemme, and M. Nemirovsky, "Graphene-enabled wireless communication for massive multicore architectures," *IEEE Commun. Mag.*, vol. 51, no. 11, pp. 137–143, Nov. 2013.
- [17] J. Murray, N. Tang, P. P. Pande, D. Heo, and B. A. Shirazi, "DVFS pruning for wireless NoC architectures," *IEEE Des. Test*, vol. 32, no. 2, pp. 29–38, Apr. 2015.
- [18] S. Abadal, A. Cabellos-Aparicio, E. Alarcon, and J. Torrellas, "WiSync: An architecture for fast synchronization through onchip wireless communication," ACM SIGPLAN Notices, vol. 51, no. 4, pp. 3–17, Mar. 2016. [Online]. Available: http://doi.acm. org/10.1145/2954679.2872396
- [19] M. S. Shamim, N. Mansoor, R. S. Narde, V. Kothandapani, A. Ganguly, and J. Venkataraman, "A wireless interconnection framework for seamless inter and intra-chip communication in multichip systems," *IEEE Trans. Comput.*, vol. 66, no. 3, pp. 389–402, Mar. 2017.
- [20] M. A. I. Sikder, A. Kodi, W. Rayess, D. DiTomaso, D. Matolak, and S. Kaya, "Exploring wireless technology for off-chip memory access," in *Proc. IEEE 24th Annu. Symp. High-Perform. Interconnects*, Aug. 2016, pp. 92–99.
- [21] N. Kirman, M. Kirman, R. K. Dokania, J. F. Martinez, A. B. Apsel, M. A. Watkins, and D. H. Albonesi, "Leveraging optical technology in future bus-based chip multiprocessors," in *Proc. 39th Annu. IEEE/ACM Int. Symp. Microarchit.*, 2006, pp. 492–503.
- [22] P. J. Quinn, "Silicon innovation exploiting Moore scaling and more than Moore technology," in *High-Performance AD and DA Converters, IC Design in Scaled Technologies, and Time-Domain Signal Processing.* Berlin, Germany: Springer, 2015, pp. 213–232.
- [23] Y. Arakawa, T. Nakamura, Y. Urino, and T. Fujita, "Silicon photonics for next generation system integration platform," *IEEE Commun. Mag.*, vol. 51, no. 3, pp. 72–77, Mar. 2013.
- [24] J. H. Lau, "Overview and outlook of three-dimensional integrated circuit packaging, three-dimensional Si integration, and threedimensional integrated circuit integration," J. Electron. Packag., vol. 136, no. 4, 2014, Art. no. 040801.

Authorized licensed use limited to: The George Washington University. Downloaded on October 24,2022 at 14:03:55 UTC from IEEE Xplore. Restrictions apply.

- [25] M. T. Wade, F. Pavanello, J. Orcutt, R. Kumar, J. M. Shainline, V. Stojanovic, R. Ram, and M. Popovic, "Scaling zero-change photonics: An active photonics platform in a 32 nm microelectronics SOI CMOS process," in *CLEO*, 2015, OSA Technical Digest, Art. no. SW4N–1.
- [26] A. González-Fernández, J. Juvert, M. Aceves-Mijares, and C. Domínguez, "Monolithic integration of a silicon-based photonic transceiver in a CMOS process," *IEEE Photon. J.*, vol. 8, no. 1, pp. 1–13, Feb. 2016.
- [27] J. S. Orcutt, B. Moss, C. Sun, J. Leu, M. Georgas, J. Shainline, E. Zgraggen, H. Li, J. Sun, M. Weaver, et al., "Open foundry platform for high-performance electronic-photonic integration," *Optics Express*, vol. 20, no. 11, pp. 12 222–12 232, 2012.
- [28] M. Hochberg and T. Baehr-Jones, "Towards fabless silicon photonics," Nature Photon., vol. 4, no. 8, pp. 492–494, 2010.
- [29] D. Schoeniger, R. Henker, S. Schumann, and F. Ellinger, "A lownoise energy-efficient inductor-less 50 Gbit/s transimpedance amplifier with high gain-bandwidth product in 0.13-µm SiGe BiCMOS," in Proc. Int. Semicond. Conf. Dresden-Grenoble, 2013, pp. 1–5.
- [30] S. Seth, C. H. J. Poh, T. Thrivikraman, R. Arora, and J. D. Cressler, "Using saturated SiGe HBTs to realize ultra-low voltage/power X-band low noise amplifiers," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meet.*, 2011, pp. 103–106.
- [31] L. Cabria, J. Garcia, E. Malaver, et al., "A PHEMT frequency doubling active antenna with BPSK modulation capability," *IEEE Antennas Wireless Propag. Lett.*, vol. 3, no. 1, pp. 310–313, 2004.
- [32] K. Kang, P. D. Dong, J. Brinkhoff, C.-H. Heng, F. Lin, and X. Yuan, "A power efficient 60 GHz 90 nm CMOS OOK receiver with an on-chip antenna," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Tech*nol., 2009, pp. 36–39.
- [33] R. Berenguer, G. Liu, A. Akhiyat, K. Kamtikar, and Y. Xu, "A 43.5 mW 77 GHz receiver front-end in 65 nm CMOS suitable for FM-CW automotive radar," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2010, pp. 1–4.
- [34] E. Seok, D. Shim, C. Mao, R. Han, S. Sankaran, C. Cao, W. Knap, and K. Kenneth, "Progress and challenges towards terahertz CMOS integrated circuits," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1554–1564, Aug. 2010.
- [35] K. KrishneGowda, R. Kraemer, A. Wolf, J. C. Scheytt, and I. Kallfass, "Wireless 100 Gb/s: PHY layer overview and challenges in the THz freqency band," in *Proc. IEEE 15th Annu. Wireless Microw. Technol. Conf.*, 2014, pp. 1–4.
- [36] P. Nenzi, F. Tripaldi, V. Varlamava, F. Palma, and M. Balucani, "On-chip THz 3D antennas," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf.*, May 2012, pp. 102–108.
- [37] M.-R. Nezhad-Ahmadi, M. Fakharzadeh, B. Biglarbegian, and S. Safavi-Naeini, "High-efficiency on-chip dielectric resonator antenna for mm-wave transceivers," *IEEE Trans. Antennas Propag.*, vol. 58, no. 10, pp. 3388–3392, Oct. 2010.
- [38] S. Pan and F. Capolino, "Design of a CMOS on-chip slot antenna with extremely flat cavity at 140 GHz," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 827–830, 2011.
- [39] B. Floyd, C.-M. Hung, and K. O, "Intra-chip wireless interconnect for clock distribution implemented with integrated antennas, receivers, and transmitters," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 543–552, May 2002.
- [40] H. Cheema and A. Shamim, "The last barrier: On-chip antennas," IEEE Microw. Mag., vol. 14, no. 1, pp. 79–91, Jan. 2013.
- [41] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77 GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.
- [42] A. Shamim, L. Roy, N. Fong, and N. Tarr, "24 GHz on-chip antennas and balun on bulk Si for air transmission," *IEEE Trans. Antennas Propag.*, vol. 56, no. 2, pp. 303–311, Feb. 2008.
 [43] S.-S. Hsu, K.-C. Wei, C.-Y. Hsu, and H. Ru-Chuang, "A 60 GHz
- [43] S.-S. Hsu, K.-C. Wei, C.-Y. Hsu, and H. Ru-Chuang, "A 60 GHz millimeter-wave CPW-Fed Yagi antenna fabricated by using 0.18-µm CMOS technology," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 625–627, Jun. 2008.
- [44] K. Kang, F. Lin, D.-D. Pham, J. Brinkhoff, C.-H. Heng, Y. X. Guo, and X. Yuan, "A 60 GHz OOK receiver with an on-chip antenna in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1720–1731, Sep. 2010.
 [45] E. Peytavit, J.-F. Lampin, T. Akalin, and L. Desplanque, "Integra-
- [45] É. Peytavit, J.-F. Lampin, T. Akalin, and L. Desplanque, "Integrated terahertz TEM horn antenna," *Electron. Lett.*, vol. 43, no. 2, pp. 73–75, Jan. 2007.

- [46] J. Balfour and W. J. Dally, "Design tradeoffs for tiled CMP on-chip networks," in Proc. 20th Annu. Int. Conf. Supercomput., 2006, pp. 187–198.
- [47] A. Kodi and A. Louri, "A system simulation methodology of optical interconnects for high-performance computing systems," J. Opt. Netw., vol. 6, no. 12, pp. 1282–1300, 2007.
- [48] J. Kim, W. J. Dally, B. Towles, and A. K. Gupta, "Microarchitecture of a high-radix router," ACM SIGARCH Comput. Archit. News, vol. 33, no. 2, pp. 420–431, 2005.



Avinash Karanth received the BE degree in electronics and communications in February 2000 from the Manipal Institute of Technology, Mangalore University, and the MS and PhD degrees in the Electrical and Computer Engineering Department from The University of Arizona in May 2003 and August 2006, respectively. Presently, he is the Joseph Jachinowski Professor in the School of Electrical Engineering and Computer Science at Ohio University in Athens, Ohio. Dr. Karanth directs the Technologies for Emerging

Computer Architecture Lab (TEAL) at Ohio University. His research interests include computer architecture, optical interconnects, Network-on-Chips (NoCs) and emerging technologies such as nanophotonics, 3D, and wireless interconnects. He is the recipient of the NSF CAREER Award in 2011, the Presidential Research Scholar Award in 2017, the Best Paper Award at the ICCD 2013 conference and his papers have been nominated for Best Paper at the IEEE Symposium on Network-on-Chips (NoCs) in May 2010 and the IEEE Asia & South Pacific Design Automation Conference (ASP-DAC) in January 2009. He is a senior member of the IEEE and member of ACM.



Savas Kaya received the PhD degree from the Imperial College of Science, Technology and Medicine, London, in 1998, for his work on strained Si quantum wells on vicinal substrates, following the MPhil degree in 1994 from the University of Cambridge on polarization insensitive liquid crystal switches. He was a post-doctoral researcher at the University of Glasgow between 1998 and 2001, carrying out research in transport and scaling in Si/SiGe MOSFETs, and fluctuation phenomena in decanano MOSFETs. He is cur-

rently a professor with the Russ College of Engineering at Ohio University, Athens. His other interests include transport theory, device modeling and process integration, nanofabrication, nanostructures, and nanosensors. He is a senior member of the IEEE.



Ashif Sikder received the BS degree in electrical engineering from the Bangladesh University of Engineering and Technology in 2012, and the MS degree in electrical engineering from Ohio University in 2016 with a research focus on computer architecture. He is currently working as an engineer at Qualcomm Atheros Inc.



Daniel Carbaugh received the BS and MS degrees in electrical engineering from Ohio University, Athens. He is currently pursuing his PhD degree in electrical engineering from Ohio University as well. His current research includes optics and photonics, specifically waveguide and micro-lens design and fabrication.



Soumyasanta Laha received MS degree in embedded digital systems with distinction from the University of Sussex, UK, in 2007 and the PhD degree in electrical engineering from the Russ College of Engineering and Technology, Ohio University, Athens, OH, USA, in 2014. He is currently an assistant professor at the Department of Electrical and Computer Engineering, California State University, Fresno, CA, USA. His research interests among others include energyefficient mm-wave/RF transceivers, and biomedi-

cal instrumentation. He has published nearly 30 papers in the above areas and has nearly five years of industry and research experience in mm-wave IC design, analog electronics, biomedical instrumentation, and embedded systems in the USA, Austria, the UK, and India. Dr. Laha was the recipient of the Stocker Research Fellowship by Ohio University.



Dominic DiTomaso received the BS, MS, and PhD degrees in electrical engineering and computer science from Ohio University, Athens, in 2010, 2012, and 2015, respectively. From 2015-2016, he was a postdoctoral researcher at Ohio University. He currently works for IBM in Poughkeepsie, NY, in the field of computer architecture.



Ahmed Louri received the PhD degree in computer engineering from the University of Southern California, Los Angeles, California in 1988. He is the David and Marilyn Karlgaard Endowed Chair Professor of Electrical and Computer Engineering at the George Washington University, which he joined in August 2015. He is also the director of the High Performance Computing Architectures and Technologies Laboratory. From 1988 to 2015, he was a professor of electrical and computer engineering at the University of Arizona,

and during that time, he served six years (2000 to 2006) as the chair of the Computer Engineering Program. From 2010 to 2013, He served as a program director in the National Science Foundation's (NSF) Directorate for Computer and Information Science and Engineering. He directed the core computer architecture program and was on the management team of several cross-cutting programs. He conducts research in the broad area of computer architecture and parallel computing, with emphasis on interconnection networks, optical interconnects for scalable parallel computing systems, reconfigurable computing systems, and power-efficient and reliable Network-on-Chips (NoCs) for multicore architectures. He has published more than 160 refereed journal articles and peerreviewed conference papers and is the co-inventor on several US and international patents. Dr. Louri's research has been sponsored by NSF, Department of Energy, Air Force Office of Scientific Research, the David and Marilyn Karlgaard Endowment Fund, and industrial corporations such as Intel, IBM, Cisco, Sun Microsystems (now Oracle), Raytheon, Physical Optics Corporation, and US West Technologies. He is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), a member of IEEE Computer Society (CS) Technical Committee on Computer Architecture, the IEEE CS Technical Committee on Parallel Processing, the IEEE CS Technical Committee on Microprocessors & Microcomputers, and the Optical Society of America.



Hao Xin (F'18) received the BS degree in physics and mathematics from the University of Massachusetts, Dartmouth, in May 1995 and the PhD degree in physics from the Massachusetts Institute of Technology in February 2001. He is a professor of electrical and computer engineering at the University of Arizona. He is named an Arizona Engineering fellow in Aug. 2013. He also served as the inaugural director of the Cognitive Sensing Center of the ECE Department at the University of Arizona. He joined the University of

Arizona since August 2005 as an assistant professor. He was promoted to tenured associate professor in 2009 and to full professor in 2012. From 2000 to 2003, he was a research scientist with the Rockwell Scientific Company in Thousand Oaks, CA. He was a Sr. principal multidisciplinary engineer with Raytheon Company in Tucson, AZ, from 2003 to 2005. His primary research interests are in the area of microwave / millimeter wave / THz antennas, devices, circuits, and their applications in wireless communication and sensing systems. He has authored over 300 referred publications and 14 patents (13 issued and 1 pending) in the areas of microwave and millimeter-wave technologies, random power harvesting based on ferro-fluidic nano-particles, and carbon nanotube based devices.



Junqiang Wu received the BS and MEng degrees in electrical engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2010 and 2013, respectively, and the PhD degree in electrical and computer engineering from the University of Arizona, Tucson, AZ, USA, in 2017. He is currently a member of technical service with Maxim Integrated Inc., Beaverton, OR, USA. He was a chapter chair of the Tucson Microwave Theory and Techniques Society Student Branch Chapter from 2015 to 2016.

▷ For more information on this or any other computing topic, please visit our Digital Library at www.computer.org/publications/dlib.