

# The Equivalency Processing Parallel Photonic Integrated Circuit (EP<sup>3</sup>IC), a Parallel Digital Equivalence Search Module

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## Abstract

*We present an optoelectronic module called the Equivalency Processing Parallel Photonic Integrated Circuit (EP<sup>3</sup>IC). EP<sup>3</sup>IC is created specifically to implement high-speed digital parallel equivalence searches (i.e. a database word search or multimedia search). The module implements a parallel computation model with multiple-wavelength photonic integrated circuit technology. Based on simulation and initial analytical computation, a single-step multiple-comparand word-parallel bit-parallel equality search can achieve an aggregate processing speed of 82 terabits per second. We outline the theoretical design of the monolithic module and integrated components, compare this with a functionally identical bulk-optics implementation. This integrated circuit solution provides relatively low-power operation, fast switching speed, a compact system footprint, vibration tolerance, and is highly manufacturable.*

## 1. Introduction

Among the integrated optoelectronic systems presently being investigated, two concepts have emerged as forerunners in the optoelectronic processor race. The first of these concepts is based on what are known as "smart pixels." [1,2,3] By the use of rudimentary electronic logic for processing and optical sources and detectors for communication, arrays of smart pixels have the capacity for the parallel manipulation of large data sets. The second concept to emerge is called the photonic processor. Here, light participates directly in the processor computation by being manipulated by various active and passive optical devices. Unlike the smart pixel approach, a photonic processor processes data at the speed of light, without the need for intermediate conversion to electronics. For example, the Fourier transform operation is naturally suited for optics and can be implemented with a

handful of lenses. Real-time image processing and correlation are two applications that are well-documented in the literature [4].

Photonic processors have also made encouraging progress in optical associative processors for database processing [5,6]. Various designs have been proposed and successfully demonstrated with free-space optics including the Optical Content-Addressable Memory (OCAM) [7] and Optical Content-Addressable Parallel Processor (OCAPP) [8] research systems, and Opticom's Digital Optical Computer II (DOC II) commercial prototype architectures [9]. The most significant demonstrations have involved the implementation of the database pattern search (equality operation) in which a search word is optically compared against several database words in parallel. However, the microsecond switching speeds of optical active elements such as spatial light modulators (SLM's) cannot realistically compete with the sub-nanosecond switching speeds of high-performance electronic transistors.

In an effort to increase the number of words that can be simultaneously compared against a database, we have been adapting a concept that has become popular in the telecommunications industry, namely wavelength-division multiplexing (WDM). WDM increases the communications bandwidth of a channel by simultaneously transmitting multiple signals within the same space, each encoded on a separate optical wavelength. Our system, called the Multi-Wavelength Optical Content-Addressable Parallel Processor (MW-OCAPP) [10], adapts this concept to optical computing systems by simultaneously processing multiple database arguments by encoding each on a separate wavelength. MW-OCAPP offers constant-time multi-comparand processing equality searching and efficient use of hardware. Additionally, MW-OCAPP is extendable to include the computation of higher-order database operations such as Magnitude Comparison [11], Union, Intersection and others. We have physically demonstrated the multiwavelength equality operation.

In an attempt to shrink the processor dimensions and dramatically enhance system performance, we have developed an integrated-optics version of MW-OCAPP. We call this new system the Equivalency Processing Parallel Photonic Integrated Circuit (EP<sup>3</sup>IC). Instead of using bulky discrete laser arrays or spatial light, EP<sup>3</sup>IC integrates laser sources, modulators, detectors, passive elements and waveguides on a single monolithic substrate. When compared with discrete optic solutions such as OCAM or MW-OCAPP, EP<sup>3</sup>IC allows for the realization of a very compact and reliable system that has low power consumption, is vibration insensitive, has a small system size and is manufacturable. Monolithic integration, also, allows for the bit comparison rates of EP<sup>3</sup>IC to far exceed that which is possible with MW-OCAPP.

## 2. Data Encoding

EP<sup>3</sup>IC, like MW-OCAPP [10] uses several methods for encoding a data-plane on a light-plane. Binary patterns are represented by spatially distributed orthogonally-polarized logic states. Logical '1' is defined as vertically polarized light and logical '0' as horizontally polarized light. The presence or absence of light (intensity threshold) within a waveguide indicates the selection or de-selection of words or attributes in the system. The Comparand Array (CA) is the data array that contains the words to be matched and the Relational Array (RA) is the main database that contains the words to match against. Individual tuples are differentiated from one another by polarization encoding each on a unique wavelength.

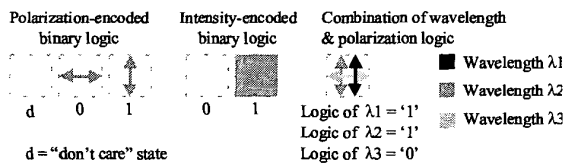


Figure 1. The optical data encoding scheme using various degrees-of-freedom (polarization and intensity).

## 3. Architectural Overview

The proposed EP<sup>3</sup>IC device is a planar structure composed of an integrated series of optical components connected by waveguides. The operating wavelength range for EP<sup>3</sup>IC corresponds to the low-loss region of optical silica-based fiber, or 1.4 to 1.65 $\mu$ m. One of the most popular systems for emitter/detectors operating at these low-loss wavelengths is the InGaAsP/InP system [12] which has a bandgap of about 1.35 eV. Using InP

as the base material, several quaternary compounds can be created with 'customized' energy gaps corresponding to the 1.0 to 1.6  $\mu$ m range. In addition to the good fundamental optical properties of InP, several optoelectronic structures have previously been integrated into this system, demonstrating its practical value. Lasers, modulators, waveguides, and detectors have all been successfully integrated on the same InP substrate [13,14,15,16,17]. There are six integrated sub-components in the EP<sup>3</sup>IC system: the distributed feedback laser (DFB), the rib waveguide structure, the active polarization mode converter, the waveguide polarization filter, the waveguide grating demultiplexer, and the photodetectors.

In order to best present the architecture of EP<sup>3</sup>IC, a side-by-side comparison is now made with the bulk optics implementation in MW-OCAPP. In the example to follow, two two-bit words in the comparand array ("10", "01") are simultaneously being compared against two two-bit words in the relational array ("01", "11"). Where appropriate, simulation and modeling results have been included from a beam propagation simulator called Prometheus [18] and a ray trace package called ASAP [19].

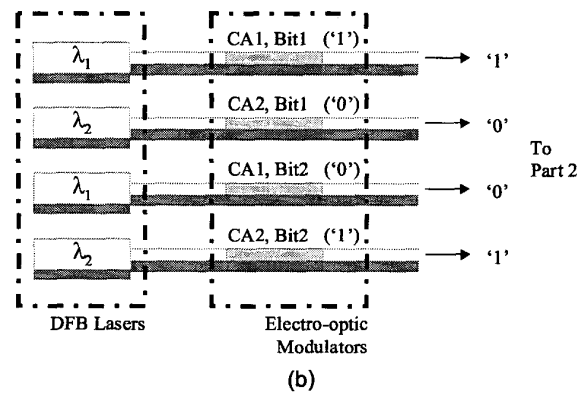
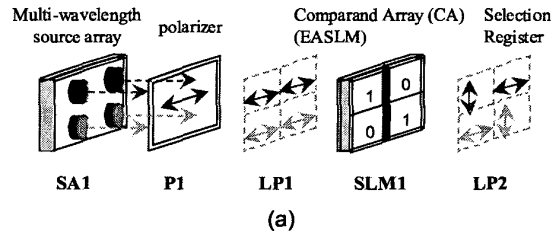


Figure 2: (a) Part 1 of MW-OCAPP's equivalency system schematic and (b) EP<sup>3</sup>IC's waveguide equivalent (SA=Source Array, P=Polarizer, SLM=Spatial Light Modulator, LP=Light Plane)

The first part of the equivalency system as found in MW-OCAPP is shown in Figure 2a. Its purpose is to encode a pixilated two-dimensional optical wavefront with the comparand array (CA) to be processed. The “rows” in the wavefront, each encoded on a unique wavelength, represent words to be matched. Polarization encoding of the desired data pattern is employed to differentiate the binary states of each of the pixilated “bits”. Using free-space optics, we begin with a multi-wavelength source array (SA1) in which each row (which corresponds to a separate tuple) radiates at a different wavelength. This wavefront passes through a horizontally-oriented polarizer (P1) to reset all of the bit positions to the ‘0’ logical state (LP1). Light-plane LP1 impinges on an electronically-addressable spatial light modulator (SLM1) which polarization-encodes the light passing through it with the comparand array bit pattern. The resultant light-plane, LP2, is called the Selection Register (SR) and represents the optically-encoded version of the comparand array.

Figure 2b illustrates EP<sup>3</sup>IC’s monolithic implementation of the architecture. The proposed substrate material used in this is EP<sup>3</sup>IC InP. The source array in this case is a distributed feedback laser (DFB) array (continuous wave operation) that radiates parallel to the substrate surface [20]. For this example, alternating lasers radiate on different wavelengths. Since DFB lasers emit light polarized in the TE orientation (parallel to the chip surface), all of the light is by default in the logical ‘0’ orientation. The lasers are coupled into a single-mode rib waveguide composed of InGaAsP that is designed to be near-isotropic [21]. The next devices in the path are a series of electro-optic modulators [22,23] that encode each of the CA words. These modulators are synchronized by a high-speed electronic host system, and operate at the system frequency of 10 GHz. The proposed electro-optic material used is a poled polymer such as PPNA or FLAMEL [24].

Figure 3a illustrates the second part of the equivalency operation for MW-OCAPP and EP<sup>3</sup>IC. Its purpose is to bit-wise exclusive-or (XOR) each tuple in the comparand array with each tuple in the relational array (RA). This produces a logical ‘1’ at every bit position where there is a CA and RA mismatch. The encoded light plane from Figure 2a (LP2) passes through a holographic optical element array which duplicates each of the rows with different wavelengths over the full surface of an EASLM (SLM2). Light plane LP3 passes through SLM2 encoded with the relational array (RA) to be searched. The EASLM rotates the polarization of the incident light according

to the logic states of its pixels, effectively generating the result of the logical XOR operation in LP4. Light plane LP4 is called the Match-Compare Register (MCR) and contains all of the bit match and mismatch locations of each of the CA and RA tuple combinations (designated by horizontally and vertically-polarized light respectively).

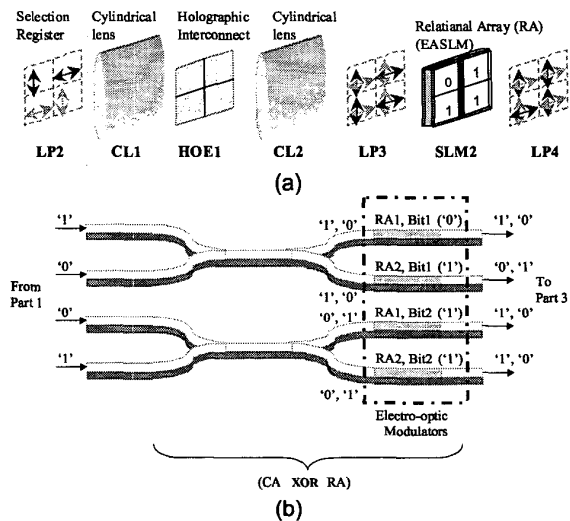


Figure 3. (a) Part 2 of MW-OCAPP’s equivalency system schematic. (b) EP<sup>3</sup>IC’s waveguide equivalent. The first state in the logic pairs following the y-splitter corresponds with  $\lambda_1$  and the second state in the pairs corresponds with  $\lambda_2$ .

Figure 3b illustrates EP<sup>3</sup>IC’s waveguide equivalent of the second part of the equivalency operation. The first and second bit positions in each of the words are mixed together using a y-coupler, and are then split using a 3 dB y-splitter. These mixed logic states pass through electro-optic modulators which are encoded with the RA pattern. The resulting light plane is the Match-Compare Register, and this passes on to Part 3.

The third and final part of the equivalency unit identifies which combinations of CA and RA tuples are matches. It does so by operating on the Match-Compare Register by converting it to a pixilated map called the Equality Register that represents the equivalency of all of the CA and RA tuple combinations.

Figure 4a illustrates the final section of the equality operation. The MCR (LP4) enters and passes through a vertically-oriented polarizer (P2) to form LP5. LP5 contains an illuminated pixel corresponding to all bit mismatch positions. LP5 is funneled down to a single column by CL3 and CL4. This single column (LP6)

must now be wavelength de-multiplexed into a plane that has a pixel count width equal to the number of tuples in the CA. This can be accomplished using a holographic element (HOE2) that is fabricated to deflect light at an angle that is a function of its wavelength. Cylindrical lens (CL5) collimates the light exiting HOE2 and produces the Equality Register (LP7).

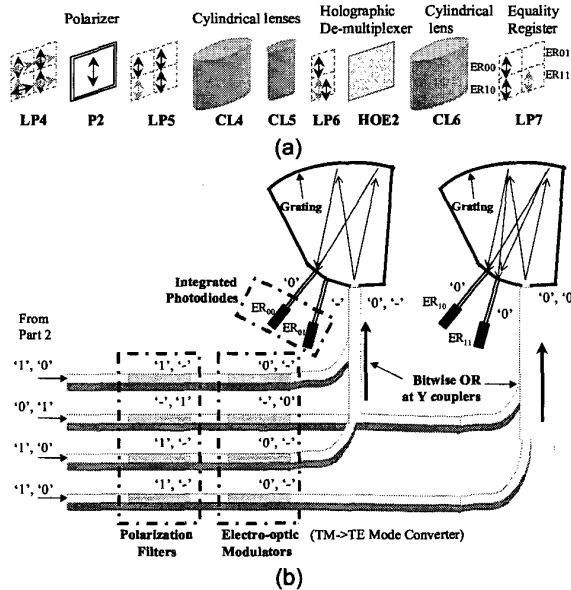


Figure 4. Part 3 of MW-OCAPP's equality system schematic (a) and EP<sup>3</sup>IC's waveguide equivalent (b). The '-' symbols following the polarization filter indicate the absence of light for a particular wavelength in a guide.

Figure 4b illustrates EP<sup>3</sup>IC's equivalent waveguide approach for the final part of the equality operation. The match-compare register from part 2 enters and passes through integrated TM-pass polarization filters. The technology chosen here is a broadband filter that utilizes a thin discontinuous silver film that is placed between the waveguide core and cladding [25]. At this point, all horizontally-polarized light (logical '0') has been filtered from each of the waveguides. This single-mode TM-polarized light for each word must now be coupled into a waveguide, performing the logical OR'ing process. A single-mode y-coupler has an inherent power loss of 3 dB [26]. One way to circumvent these power losses is to couple into a multi-mode guide where insertion losses are far less. However, making the waveguide multi-mode for TM light would involve increasing the height of the guide. This is undesirable as it increases the complexity of the

design and would cause other coupling difficulties at the detector. Therefore, a waveguide multi-mode for TM light is chosen.

Following coupling into the multi-mode waveguides, the light is separated into individual wavelengths using a vertical-walled waveguide grating spectrometer [27]. A 2mm-long device provides adequate separation for 32 channels at the wavelength range of interest. These individual channels are coupled into multi-mode waveguides that route the light to integrated photodetectors. The photodetectors used are vertically-coupled PIN diodes [28] with a matching buffer layer [29]. As in the bulk MW-OCAPP system, the photodetectors are recording the components of the Equality Register vector.

Decoding this Equality Register light plane is fairly simple. The light-plane is a two-dimensional representation of the intersection of the CA and RA. If 'n' represents the number of tuples in the CA and 'm' represents the number of tuples in the RA, then the ER must consist of  $m \times n$  pixels. It is encoded in "negative logic" meaning that non-illuminated pixels correspond to exact matches. For an  $m$  by  $n$  ER grid, pixel<sub>l,m</sub> is illuminated such that tuple RA<sub>m</sub> is not-equal-to tuple CA<sub>n</sub>. The proposed system schematic for EP<sup>3</sup>IC is illustrated in Figure 5. This configuration has an approximate footprint of 0.32cm<sup>2</sup>.

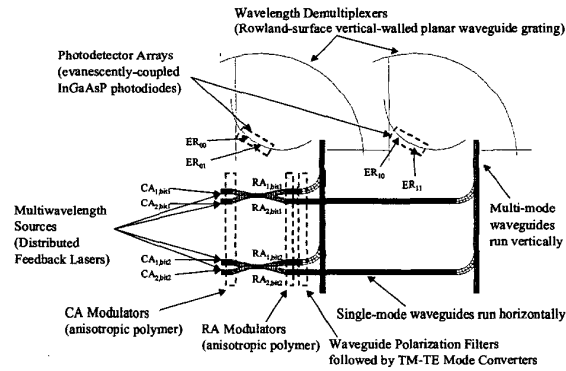


Figure 5. EP<sup>3</sup>IC Layout for a configuration consisting of two RA words, two CA words and two bits per word (ASAP model)

Figure 6 illustrates the generalized method by which EP<sup>3</sup>IC can be extended given 'm' CA words, 'q' RA words and 'n' bits per word.

#### 4. EP<sup>3</sup>IC performance Analysis

To evaluate whether the EP<sup>3</sup>IC system will function properly, a power analysis can be done. The analysis

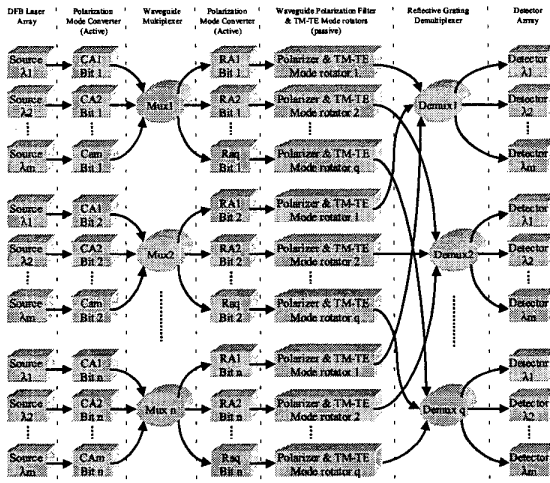


Figure 6: Functional layout of EP<sup>3</sup>IC's generalized monolithic equality processing core.

starts at the detector and works backwards along the beam path through the waveguide components and ending ultimately at the source. Each of the photodetectors require about 1  $\mu$ W of optical power in order to maintain a signal-to-noise ratio of two. Therefore, 1 $\mu$ W is the minimum amount of power that is to remain once all of the system losses are taken into account. Based on initial analysis, there is a -39.4 dB drop in power that is caused by EP<sup>3</sup>IC's various components. An input optical power of 10 mW is reduced to 1.2 $\mu$ W by the time it reaches the detector. This is sufficient to produce an SNR of about 3 at the detector. The external quantum efficiency of the sources is about 38% which means that each laser source will require 26.3 mW of input electrical power to deliver 10 mW of output optical power. The total electrical power required for all lasers is simply the product of the power per laser, the number of words in the CA, and the number of bits per word, or 26.9W. All other sources of power consumption are insignificant when compared to the laser sources, so the average electrical power consumption for this configuration of EP<sup>3</sup>IC is about 27 W. The peak bit comparison rate of the proposed example system is approximately 82 terabits per second (Tb/s).

The bit error rate (BER) for EP<sup>3</sup>IC can be estimated by referring to Figure 7. If we assume an SNR value of 2 corresponds to a digital "1" and an SNR of 1 corresponds with a "0", the corresponding optical powers can be read from the plot. A digital "1" is approximately 1 $\mu$ W and a "0" is about 0.7  $\mu$ W. For this design running at 10 GHz, the computed BER per detector is 3.6e-11. The total BER, taking into account

all detectors (32 x 8), is 9.2e-9. However, since EP<sup>3</sup>IC's word-comparison rate is on the order of 2.6\*e12 per second, there would be over 92 word-comparison errors per second at the detector. Clearly, error correction would be necessary in this case. Reducing the operating frequency to 5 GHz or increasing the power per source to 11.4mW causes the BER per detector to drop to 7e-20. The aggregate error rate for all detectors is then 1.75e-20. The number of word comparison errors per second is a mere 9.1e-8 at 5 GHz operation.

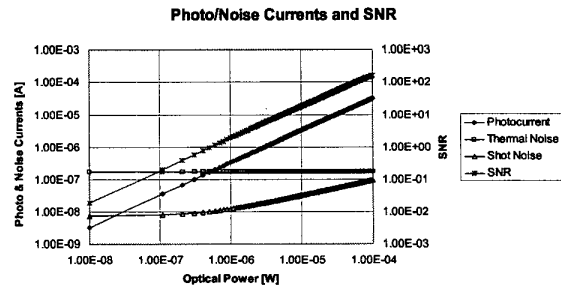


Figure 7. Analytically-derived signal-to-Noise Ratio (SNR), photo and noise currents as a function of incident optical power. A minimum SNR of 2 requires a power of 1  $\mu$ W at the photodetector.

A major obstacle that may hamper EP<sup>3</sup>IC's high-speed processing potential is in the communication link with the electronic host system. The current state-of-the-art in commercial electrical peripheral bus speed is approximately 400 MHz [30]. The aggregate input/output (I/O) transfer rate using a 64-bit-wide bus is 25.6 Gb/sec. Although fast by today's computing standards, this pales in comparison to EP<sup>3</sup>IC's communication I/O bandwidth requirements of 15.4 Tb/sec (12.8 Tb/sec input and 2.6 Tb/sec output). Obviously there would be a severe I/O bottleneck if an electrical bus were used. To eliminate the bottleneck, the equivalent electrical bus would require an impossible width of 38,500 bits! A higher-bandwidth interconnection fabric is required: optical interconnects.

Given an optical modulation rate of 10 GHz, an optical bus width of 1,540 bits (one bit per fiber) would be required to alleviate the bottleneck. Signal multiplexing using multiple wavelengths can further reduce the number of fibers required. If ten wavelengths (each modulated by a separate channel) are multiplexed per fiber, the number of required fibers reduces to 154.

Figure 8a illustrates the proposed inter-chip communications layout. The primary link consists of fiber interconnections that are butt-coupled to linear source and detector arrays at the cleaved edges of the EP<sup>3</sup>IC substrate. This approach requires no significant

device additions to the manufacturing process, since the planar sources waveguides and detectors are already present and optimized within the EP<sup>3</sup>IC architecture.

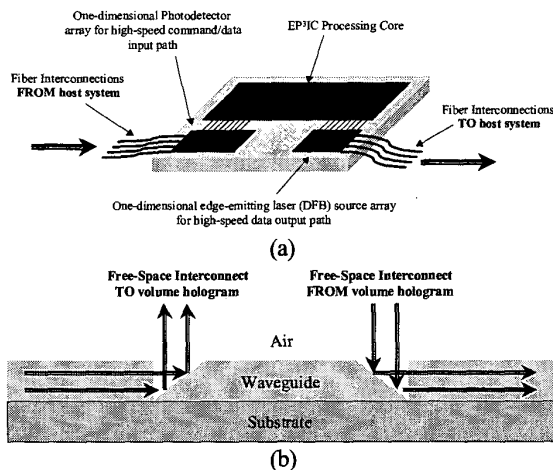


Figure 8: Proposed inter-chip input/output communication layout using fiber interconnects (a). A waveguide mirror coupler (b) could be used to realize free-space optical interconnects between the EP<sup>3</sup>IC processor and other components. This is ideally suited for high-speed parallel interfacing with optical memory such as a page-oriented volume hologram.

Interfacing EP<sup>3</sup>IC with page-oriented holographic memory for purely optical input and output is made possible by utilizing waveguide mirror-couplers [31]. The 45° angled facets permit light to be coupled into and out of the planar waveguide from normal incidence. It is conceivable that a two-dimensional array of such couplers could be arranged on the EP<sup>3</sup>IC substrate to facilitate parallel interfacing with an optical memory device. Table 1 lists a summary of EP<sup>3</sup>IC's performance parameters.

Table 1: EP<sup>3</sup>IC Performance Summary

Device Footprint	0.8 cm <sup>2</sup>
Material System	InP
Electrical Power Consumption (processor)	27 W
Peak bit comparison rate	82 Tb/sec
Input Bandwidth Requirement	12.8 Tb/sec
Output Bandwidth Requirement	2.6 Tb/sec
Laser source operating range	1.40 – 1.65 μm
System Bit Error Rate	1.2e-9

## 5. Conclusion

In this paper, we have presented an architectural design called EP<sup>3</sup>IC that combines the superior optical

parallelism present in MW-OCAPP with the processing speed and manufacturability that photonic integrated circuits allow. The proposed configuration of EP<sup>3</sup>IC (32 comparand words, 8 database word, and 8 bits per word) has a theoretical peak bit comparison rate of 82 Tb/sec and an average electrical power consumption of 27W. Ongoing work in this project includes the incorporation of logic devices in EP<sup>3</sup>IC to facilitate I/O operations. Additional efforts include an investigation into the integration of higher-order database operations as well as seeking-out additional applications that would be suitable for an EP<sup>3</sup>IC-like device. Device fabrication and prototyping is, also, under investigation.

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