Y-Junction based addressing in Optical Symmetric Multiprocessor Networks

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1. Introduction

In a symmetric multiprocessor (SMP), every processor has its own cache, and all the processors and memory modules are connected to the central interconnect, which is usually a shared bus. As the processors become faster, the central interconnect architecture of traditional SMP's impedes performance because it cannot keep up with the processors capabilities. As SMP's have hardware-enforced cache coherence, the snoop bandwidth required for address translation becomes the bottleneck. The growing performance gap between the processor speed and the conventional metal interconnection technology provides the impetus to look at optical technology for solutions. The emerging feasibility of optical interconnects is very promising for signal transmission in digital systems with high data rates at the board level and backplane. This paper proposes an architecture, which is based on scalable binary tree consisting of splitter/combiners for address translation of optical SMP. 1x4 splitters at board level and 1x8 splitters at backplane were designed and simulated using the BPM simulator Prometheus developed by Kymata Software [1].

2. Address Translation Architecture

Optical bus based multiprocessors where processors can simultaneously insert address requests was reported in [2], but in this architecture there is no provision for sharing of data among the processors as the requests are not broadcast. Star coupler has been used in [3], for broadcasting the addresses for writes using snoopy protocols and point-to-point communication for reads. This leads to additional overhead of maintaining the directory for every cache block and moreover, star coupler is used which is not easily scalable. Hence we propose a scalable binary tree consisting of dual Y-junction splitter/combiner for on-board and backplane interconnection. Optic fibers are used to connect the individual boards to the backplane as shown in figure 1. The splitter/combiner is a dual Y-junction, with the upstream Y-coupler used to combine requests from the processors to the amplifier and the downstream Y-splitter to broadcast the address request to all the modules. This enables broadcasting of memory accesses and hence the requests are serialized when seen by the processors and the memory modules. Optical time division multiplexing is used to serialize the requests, where every processor sends a request during one clock cycle. The addresses are snooped by the processors and the memory modules and appropriate action is taken. Using semiconductor optical amplifier at the root of the tree, which boosts the signal offsets the loss associated with the splitters/couplers. Vertical cavity semiconductor amplifiers at 1.3μm provide a gain of 13dB was reported in [4].

3. Design and Simulation

Ridge waveguide with a core width of 5μm having a refractive index n_{co} 1.505 and cladding having a refractive index n_{cl} 1.5 were designed using Prometheus. The structure of the 1x8 splitter/coupler for backplane is shown in figure 2. Symmetric Y-junctions for star couplers were designed in [5] show that the best results were obtained when the ending width of the splitter is half the starting width. In order to keep the width of the waveguide constant a parabolic taper section Lp of 125μm having starting width as 5μm and ending width as 10μm was added between two splitter sections. The total dimension of the structure is 6.375mm x 320μm. The separation between the output arms of the splitter were 45μm. The design ensured that the structure is single mode at 1.32μm and 0.98μm. The length of the first splitter L_1 was 3.4mm, second splitter L_2 was 1.7mm and the third splitter L_3 was 0.9mm. The splitter was composed of two S-bends of identical radii of curvature. The radius of curvature of the first splitter R_1 was 29.9mm, R_2 was 17.1mm and R_3 was 12.2mm.

The result of the simulation of 1x8 splitter at 5μm core is shown in figure 3. A loss of 8.325dB was observed in this structure. This loss is less than the 9dB fundamental loss of conventional splitters. 8x1 coupler was also designed using the same structure by exciting one of the input arms. A loss of 6.532dB was observed. The width of the core section was changed to 6.5μm, 10μm and 20μm. All the structures were now multimode at 1.32μm. The losses were identical to the loss at 5μm.

1x4 splitter was designed with the same values of L_1 ,L_2 ,R_1 ,R_2 ,the total dimension was 5.35mm x 275μm. The result of the simulation is showed in figure 4. It showed a loss of 6.53dB.

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4. Conclusion

In this paper we have focused on the main scaling issues associated with symmetric multiprocessor architectures. As a solution, we have devised an optical binary tree architecture based on optical time division multiplexing consisting of dual Y-junction splitter/combiner for backplane and on-board interconnections. We have shown the design of 1x8 splitter with loss of 8.325dB for backplane and 1x4 splitters with losses of 6.53dB for on-board interconnection. This optical SMP network provides distinct performance and cost advantages over traditional electronic interconnect and even over other optical interconnection networks.

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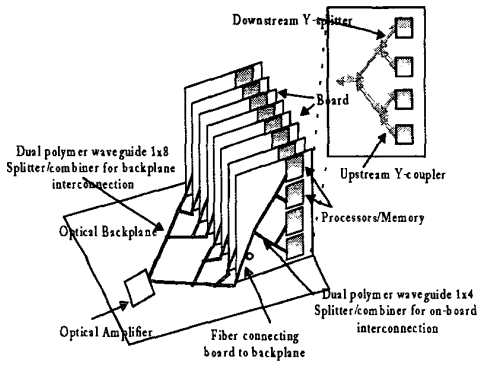

Figure 1: Processors/Memory modules connected using dual polymer splitter/combiner for on-board interconnection.Individual boards connected to splitter/combiner for backplane interconnection through fibers.

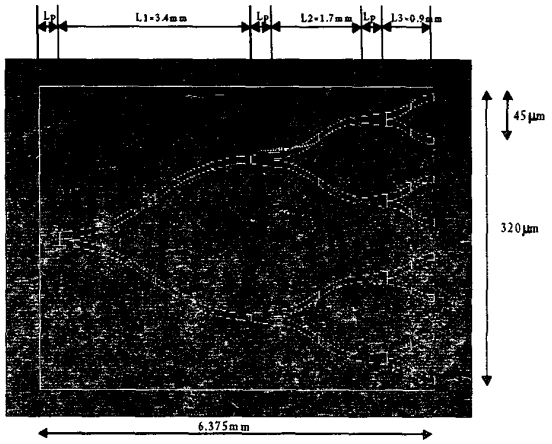

Figure 2: Structure of 1x8 splitter consisting of parabolic taper and S-bends

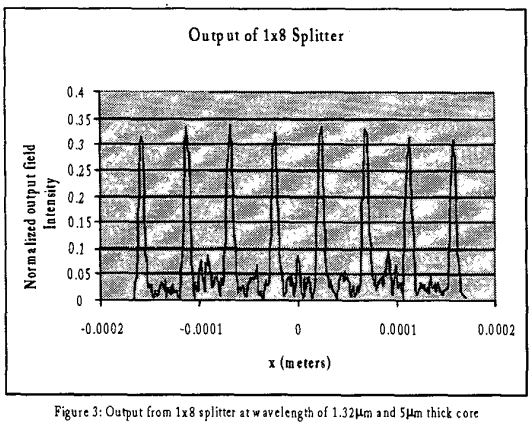

Figure 3: Output from 1x8 splitter at wavelength of 1.32μm and 5μm thick core

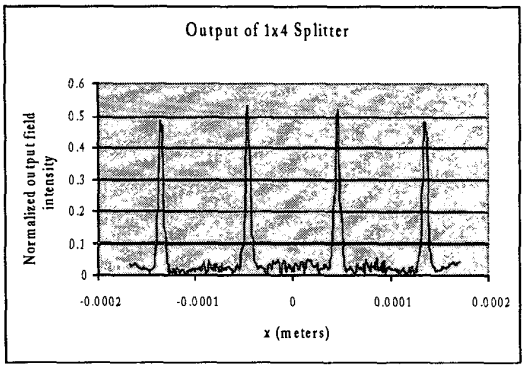

Figure 4: Output from 1x4 splitter at wavelength of 1.32μm and 5μm thick core